The Department of Electrical and Computer Engineering Presents

A DISTINGUISHED SEMINAR

PROFESSOR DEAN TULLSEN



INSTRUCTION SET ARCHITECTURE AS A LEVER FOR BETTER SECURITY, PERFORMANCE, AND EFFICIENCY IN GENERAL PURPOSE PROCESSORS

ABSTRACT \ \ \ \ \

In general purpose processors, the instruction set architecture changes little over time, to maximize software compatibility. In this talk, I make the case that abandoning that approach can provide big gains in performance, efficiency, and security without actually impacting software compatibility. I will discuss a couple of different ways to do this, potentially changing the ISA at the millisecond, microsecond, or even cycle granularity. The first is heterogeneous-ISA multicore architectures, where threads freely move between cores that run completely different ISAs, taking better advantage of diversity in the instruction stream than previous single-ISA heterogeneous architectures. I will also discuss context-sensitive decoding, which leverages the external ISA to micro-op (internal ISA) translation that happens in the decoder. By making that previously static translation dynamic, possibly changing every few cycles, we can instantly transform the instruction stream to change security levels, add performance features, etc.

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Dean Tullsen is a professor and chair of the computer science and engineering department at University of California, San Diego. He received his PhD from the University of Washington in 1996, where he introduced simultaneous multithreading (hyper-threading). He has continued to work in the area of computer architecture and back-end compilation, where with various co-authors he has introduced many new ideas to the research community, including threaded multipath execution, symbiotic job scheduling for multithreaded processors, dynamic critical path prediction, speculative precomputation, heterogeneous multi-core architectures, conjoined core architectures, event-driven simultaneous code optimization, and data triggered threads. He is a Fellow of the ACM and the IEEE. He has twice won the Influential ISCA Paper Award.

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