A word on notation. The highest voltage on chip is referred to as $V_{dd}$. The lowest voltage is referred to as $V_{ss}$.

1. (10 pts) Draw the layout of a PMOS FET for an n-well process as described in the text, lecture notes, and lab. Label each layer.

2. (10 pts) Underneath and aligned to the layout, draw the FET cross-section along a line from the source to the drain.

3. (10 pts) In the cross section from question 2, draw in the parasitic diodes.

4. (10 pts) Considering the parasitic diodes, should the n-well be tied to $V_{ss}$, $V_{dd}$, or left floating? Why?

5. (10 pts) Using parameters for the CN20 process from App. A (Table A.7) of the text, what is the maximum, minimum, and typical resistance of a minimum width x 100 $\mu$m long n-well resistor? For minimum width, see design rules in App. A.3.

6. (10 pts) What is the typical delay time through a minimum width 100$\mu$m long Poly1 resistor for the CN20 process of App. A of the text? Use typical values from (Tables A.3) for the fringe and area capacitance of Poly1 to substrate and Table A.7 for the sheet resistance of Poly1. For the minimum width, see the design rules in App. A.3.