Topics

- Design rules and fabrication.
- SCMOS scalable design rules.
- Stick diagrams.

Why we Need Design Rules

- Masks are tooling for manufacturing.
- Manufacturing processes have inherent limitations in accuracy.
- Design rules specify geometry of masks which will provide reasonable yields.
- Design rules are determined by experience.

Manufacturing Problems

- Photoresist shrinkage, tearing.
- Variations in material deposition.
- Variations in temperature.
- Variations in oxide thickness.
- Impurities.
- Variations between lots.
- Variations across a wafer.

Transistor Problems

- Variations in threshold voltage:
  - oxide thickness;
  - ion implantation;
  - poly variations.
- Changes in source/drain diffusion overlap.
- Variations in substrate.

Wiring Problems

- Diffusion: changes in doping -> variations in resistance, capacitance.
- Poly, metal: variations in height, width -> variations in resistance, capacitance.
- Shorts and opens:

Oxide Problems

- Variations in height.
- Lack of planarity -> step coverage.
Via Problems
- Via may not be cut all the way through.
- Undersized via has too much resistance.
- Via may be too large and create short.

MOSIS SCMOS Design Rules
- Designed to scale across a wide range of technologies.
- Designed to support multiple vendors.
- Designed for educational use.
- Ergo, fairly conservative.

λ and Design Rules
- λ is the size of a minimum feature.
- Specifying λ particularizes the scalable rules.
- Parasitics are generally not specified in λ units.

Wires
- metal 3
- metal 2
- metal 1
- pdiff/ndiff
- poly

Transistors

Vias
- Types of via: metal1/diff, metal1/poly, metal1/metal2.
Metal 3 via
- Type: metal3/metal2.
- Rules:
  - cut: 3 x 3
  - overlap by metal2: 1
  - minimum spacing: 3
  - minimum spacing to via1: 2

Tub Tie
- 4

Spacings
- Diffusion/diffusion: 3
- Poly/poly: 2
- Poly/diffusion: 1
- Via/via: 2
- Metal1/metal1: 3
- Metal2/metal2: 4
- Metal3/metal3: 4

Overglass
- Cut in passivation layer.
- Minimum bonding pad: 100 µm.
- Pad overlap of glass opening: 6
- Minimum pad spacing to unrelated metal2/3: 30
- Minimum pad spacing to unrelated metal1, poly, active: 15

Stick Diagrams
- A stick diagram is a cartoon of a layout.
  - Does show all components/vias (except possibly tub ties), relative placement.
  - Does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

Stick Layers
- metal 3
- metal 2
- metal 1
- poly
- ndiff
- pdiff
Dynamic Latch Stick Diagram

Sticks Design of Multiplexor

Start with NAND gate:

NAND Sticks

One-bit Mux Sticks

Layout Design and Analysis Tools

- Layout editors are interactive tools.
- Design rule checkers are generally batch---identify DRC errors on the layout.
- Circuit extractors extract the netlist from the layout.
- Connectivity verification systems (CVS) compare extracted and original netlists.
Automatic Layout

- Cell generators (macrocell generators) create optimized layouts for ALUs, etc.
- Standard cell/sea-of-gates layout creates layout from predesigned cells + custom routing.
  - Sea-of-gates allows routing over the cell.