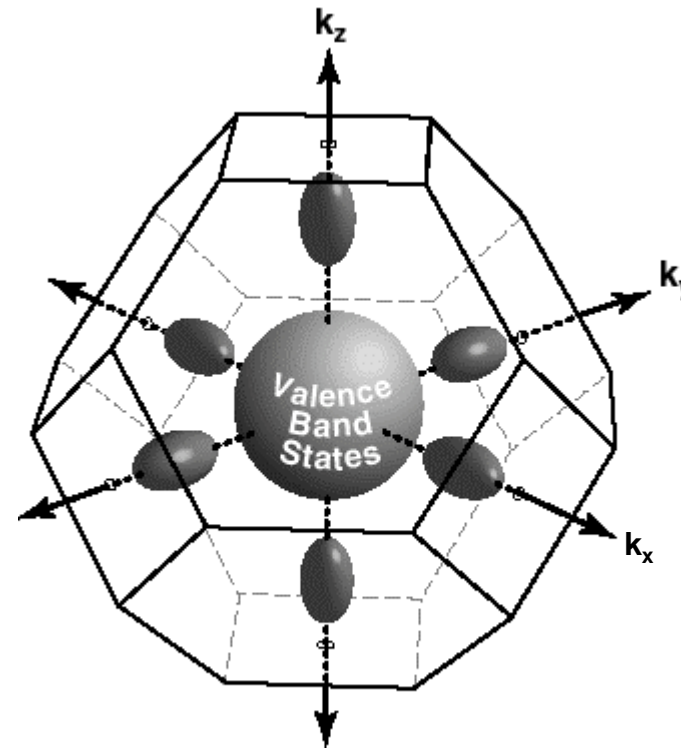
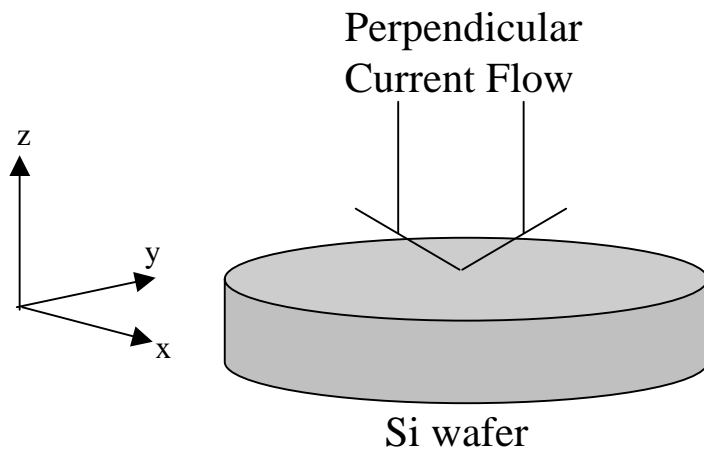


# Si - Based Tunnel Diode Operation and Forecasted Performance

Roger Lake  
Raytheon Systems  
Dallas, TX

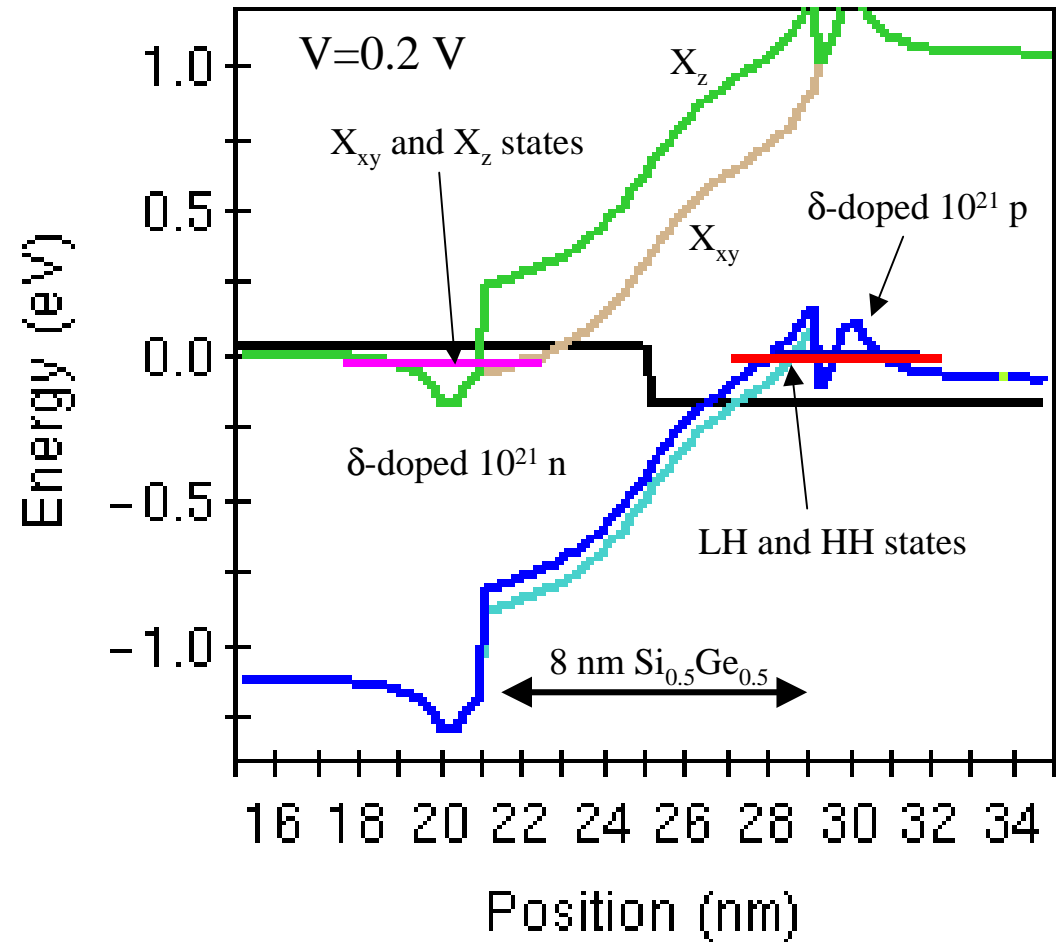
## Si / Si<sub>x</sub>Ge<sub>1-x</sub> Interband Tunnel Diodes

- The main tunneling process is LA and TO phonon assisted tunneling from the  $k_x$  and  $k_y$  electron X-valleys to the hole  $\Gamma$ -valley.
- The direct tunneling of the  $k_z$  electrons is negligible since their mass in the tunnel direction is 4 times that of the  $k_{xy}$  electrons resulting in twice the decay constant.



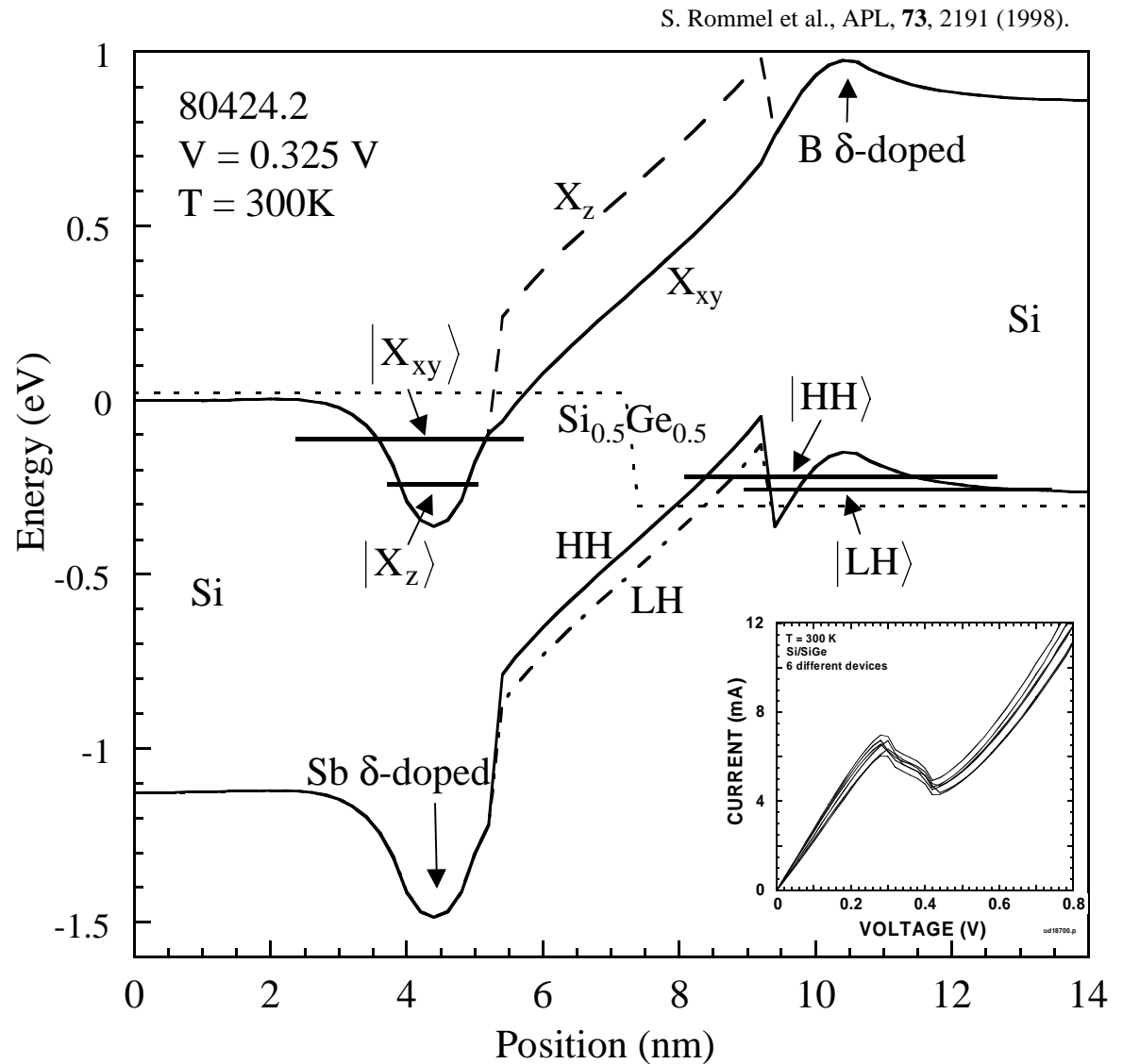
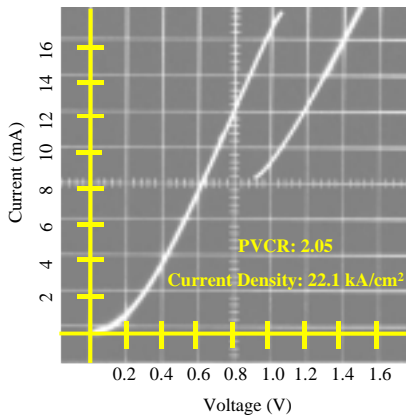
## Si / Si<sub>0.5</sub>Ge<sub>0.5</sub> Tunnel Diode Design as of 4/98

- Two items that we will change.
- 8 nm Si<sub>0.5</sub>Ge<sub>0.5</sub>
- Doping throughout Si<sub>0.5</sub>Ge<sub>0.5</sub>



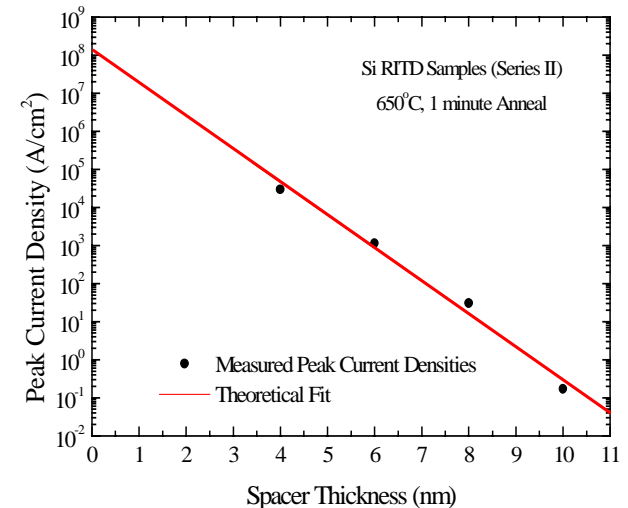
### First Working Design

- First working design built 5/98 shown at right.
- Since then, improvement has been rapid.
- A peak-to-valley-current-ratio (PVCRR) of 4.2 with a current density of 3 kA/cm<sup>2</sup> has been achieved with this exact design substituting P doping for Sb (R. Dushel et al., Electronics Lett., 35, 1111 (1999)).
- Cutting the length of the Si<sub>0.5</sub>Ge<sub>0.5</sub> region down from 4nm to 2nm, a current density of 22.1 kA/cm<sup>2</sup> with a PVCRR of 2 was obtained shown below. (S. Rommel et al., 1998 IEDM Technical Digest (IEEE, New York, 1998) p. 1035.)



### Figures of Merit - Speed Index

- High speed switching applications, the Speed Index is the important figure of merit [1].
- Speed Index =  $I_p / C$  (volts / second) where C is the tunnel diode capacitance and  $I_p$  is the peak current.
- Optimization
  - C *linearly* increases as tunnel junction width is reduced.
  - $I_p$  *exponentially* increases as tunnel junction width is reduced.
  - ==> Minimize tunnel junction width and maximize current  $I_p$ .
  - C *linearly* increases with dielectric constant  $\epsilon_{Si} = 11.9$ ;  $\epsilon_{Ge} = 16.0$ .
  - $I_p$  *exponentially* increases as bandgap decreased,  $E_{GSi} = 1.12$  eV;  $E_{GGe} = 0.66$  eV.
  - ==> Maximize  $I_p$  using  $Si_xGe_{1-x}$  tunnel region.
- For a 3.5 nm spacer with  $10^5$  A/cm<sup>2</sup> peak current (see figure right), the speed index is calculated to be 30 V GHz, i.e., 1 V can be switched at 30 GHz.

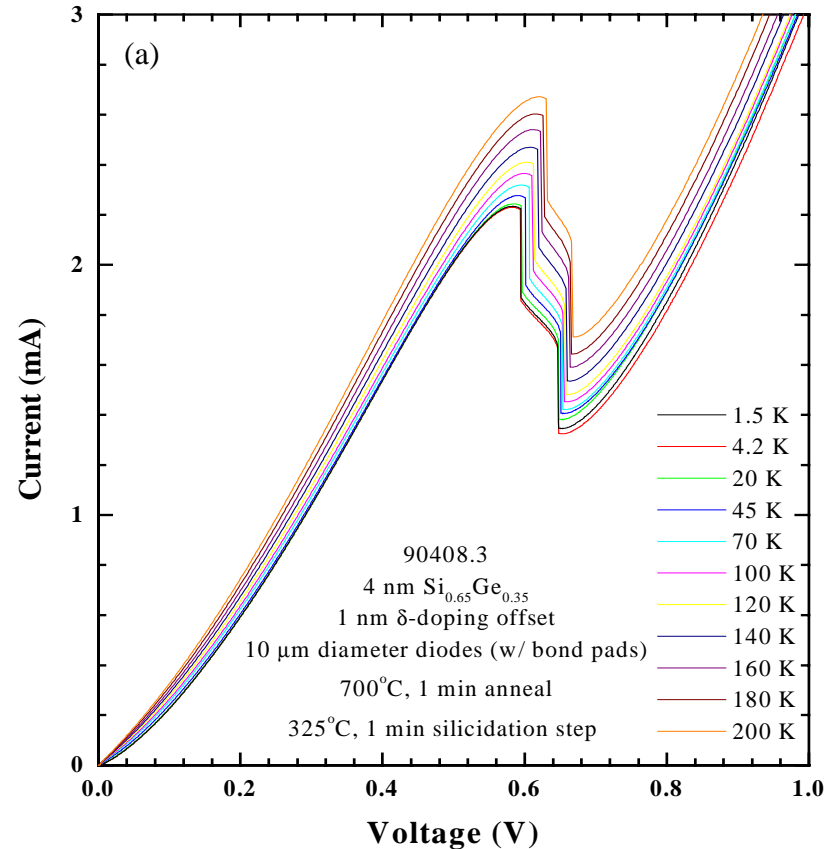


Current density vs. intrinsic-spacer thickness (S. Rommel, PhD thesis, U. Del. 1999).

[1] A. Seabaugh and R. Lake, 'Tunnel Diodes,' in Encyclopedia of Appl. Phys., Vol. 22 (Wiley-VCH, NY, 199) p. 335.

## Figures of Merit - Peak to Valley Current Ratio (PVCR)

- Both the peak currents and valley (excess) currents are tunnel currents. They are not thermally activated (see figure (a)).
- The physical mechanisms governing the valley current are still not understood.

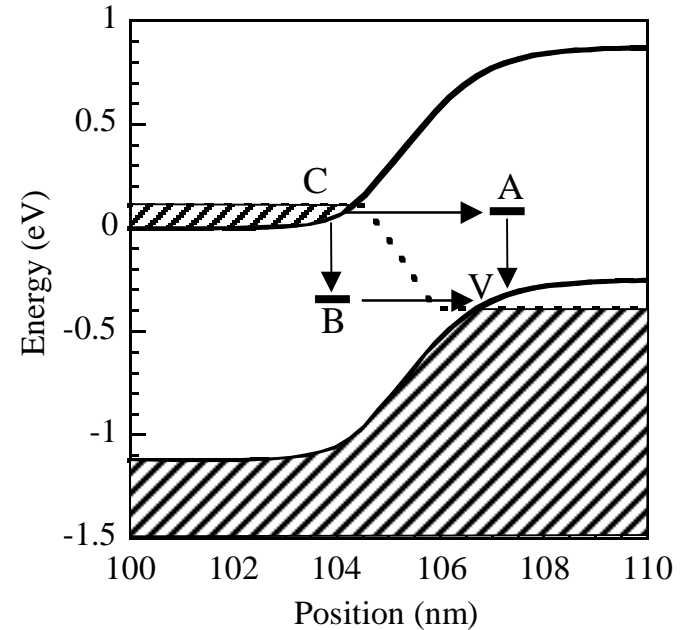
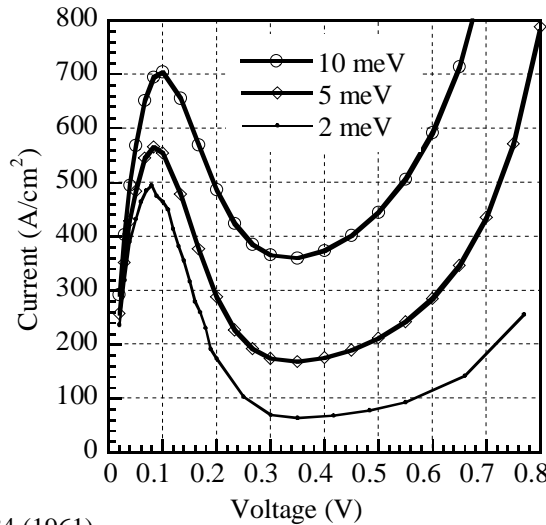
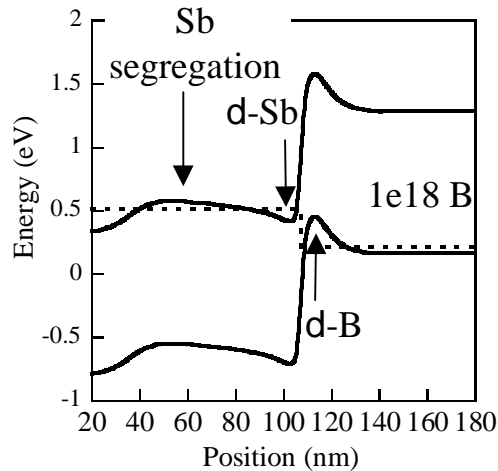


(a) Temperature dependence of tunnel current.

S. Rommel, PhD thesis, U. Del. 1999.

# Figures of Merit - Peak to Valley Current Ratio (PVCR)

- Tunneling from and through band-tails resulting from the heavy doping is one likely mechanism for the excess current [1].
- Optimization
  - Keep dopants out of the tunnel region.
- A PVCR of 4.2 has already been published and further optimization is highly probable.
- It is not yet possible to give a realistic maximum theoretical value.
- Our numerical calculations (see below) show the PVCR increasing from 1.9 to 3.4 to 7.7 as the bandtails are reduced by a factor of 2 and 2.5. Note that all of the current in figure (b) is tunnel current - not thermally activated p-n diode current. Also, compare with Fig. 4. of [1].



Excess current mechanism

## Calculated I-Vs with band-tails.

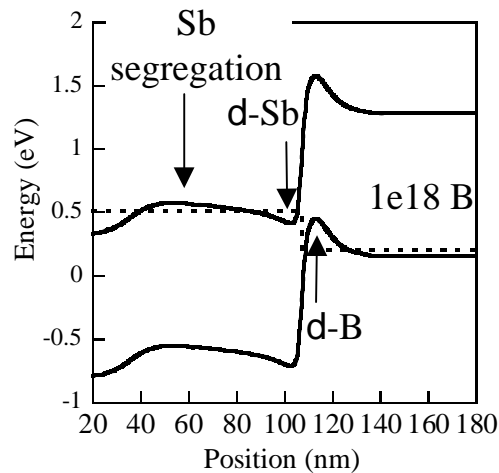
- 2nd neighbor  $sp^3s^*$  band model.
- Direct, TA, and TO phonon-assisted tunneling.
- Non-equilibrium Green function approach.

C. Rivas et al., unpublished.

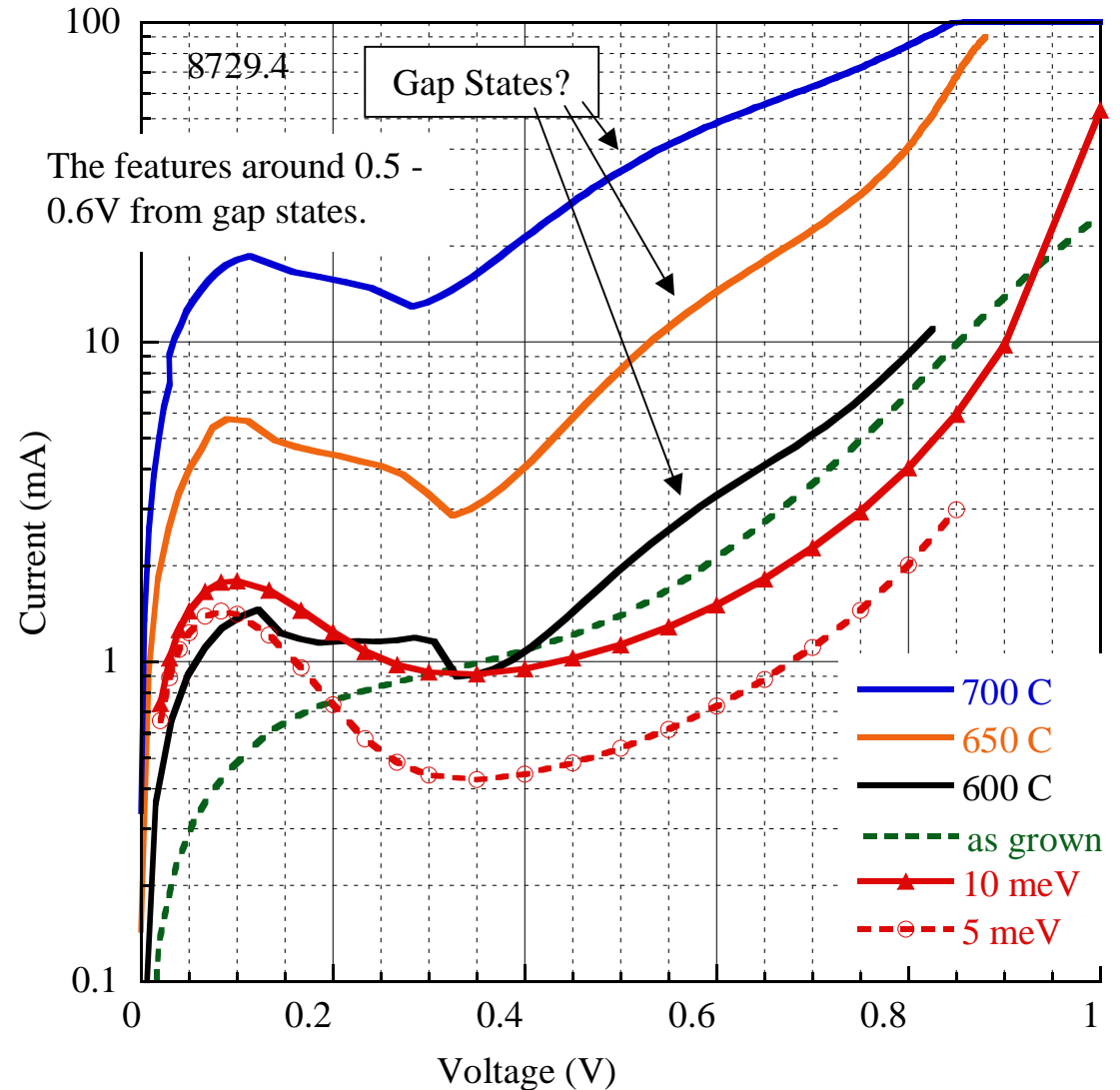
[1] Chynoweth, Feldman, and Logan, Phys. Rev., **121**, 684 (1961).

# Figures of Merit - Peak to Valley Current Ratio (PVCR)

- Low T grown heavily doped Si and  $\text{Si}_x\text{Ge}_x$  need to be understood (or at least empirically characterized).



## Gap States



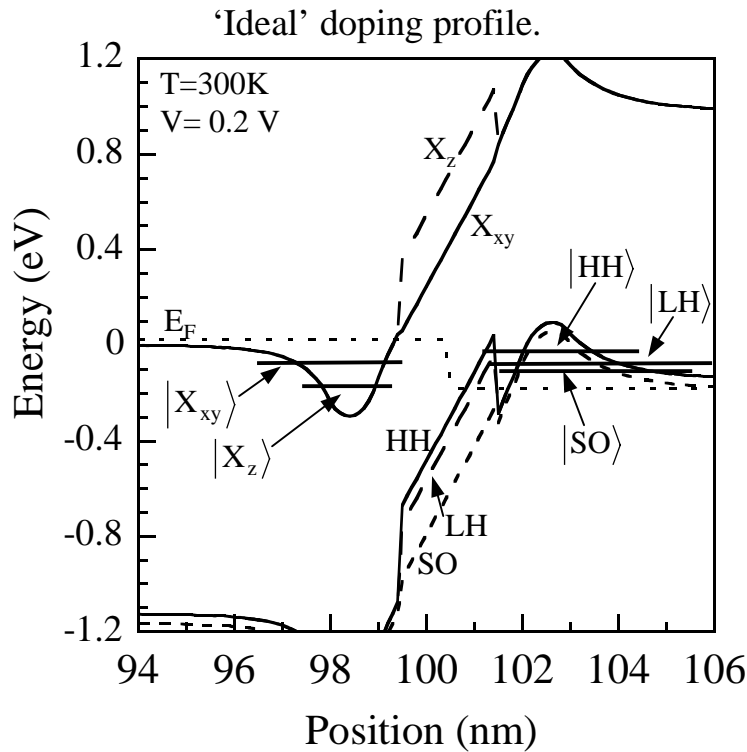
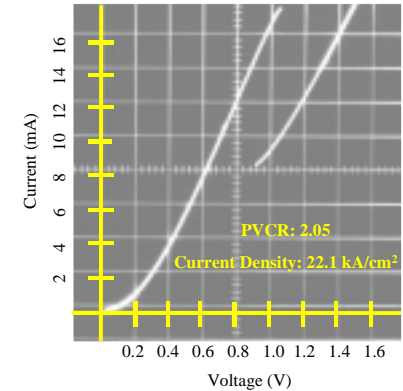
P. Thompson et al., Appl. Phys. Lett., **75**, 1308 (1999)

# Key to Optimization of both Peak and Valley Currents - Precise Control of Dopant Profiles

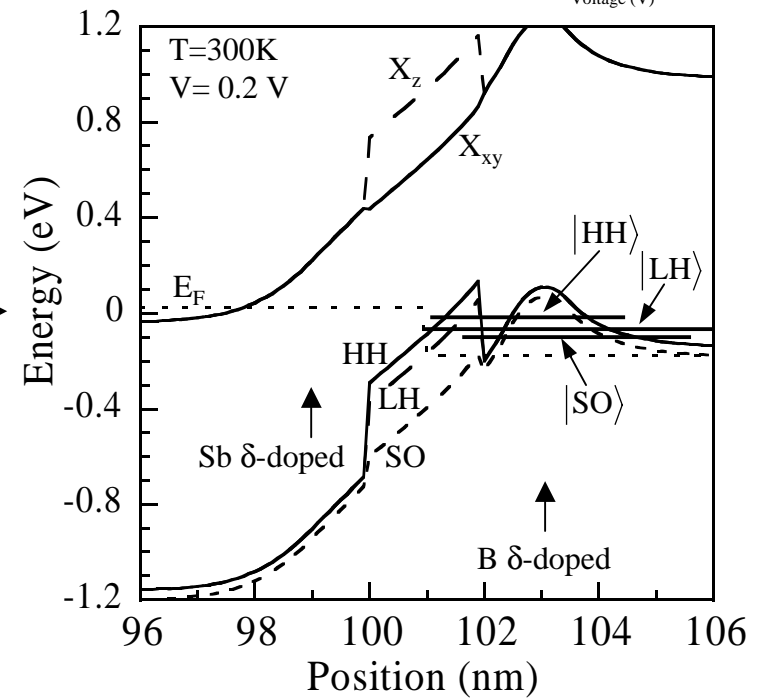
## Effect of Sb segregation

- The Sb segregates towards the surface resulting in
  - Wider tunnel barrier => Lower current density
- Opportunity for higher peak current densities by confining the Sb.
 

NB: Peak current is *exponentially* dependent on the tunnel barrier width.



Using SIMS doping data

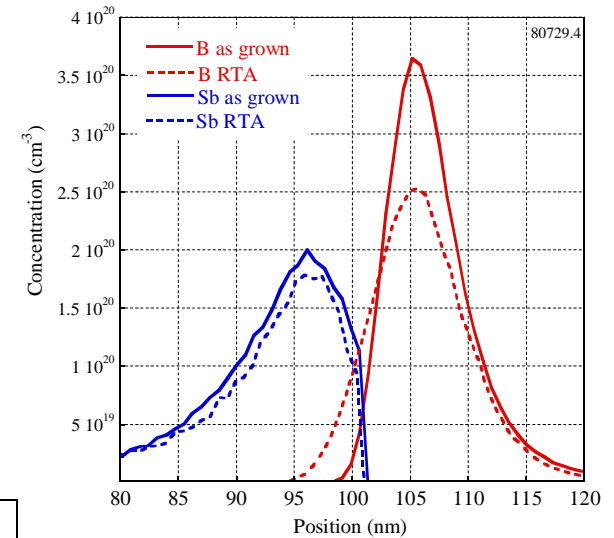
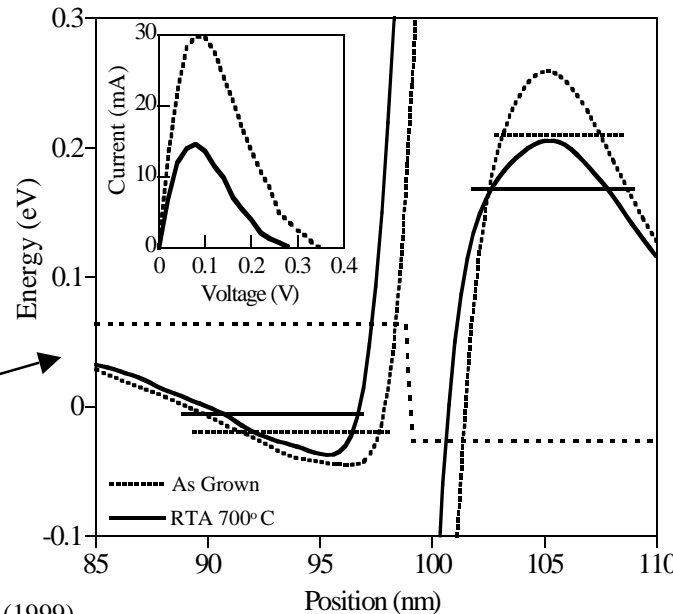
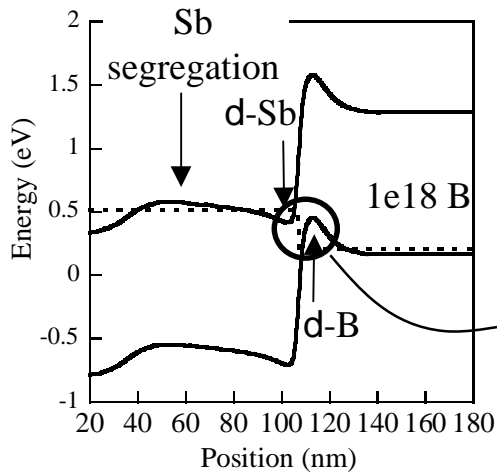


S. Rommel et al., 1998 IEDM Technical Digest (IEEE, New York, 1998) p. 1035.

# Key to Optimization - Precise Control of Dopant Profiles

## Effect of B diffusion

- As dopants diffuse and compensate, the tunnel barrier widens; the speed index and PVCR are reduced.
- Maximize PVCR by keeping dopants out of the tunnel region.
- Maximize speed index by minimizing the length of the tunnel region.
- ==> Together this implies huge doping gradients.
- Consider diffusion barriers.
- Compare different dopant species.



Dopant profiles before and after rapid thermal anneal [1].

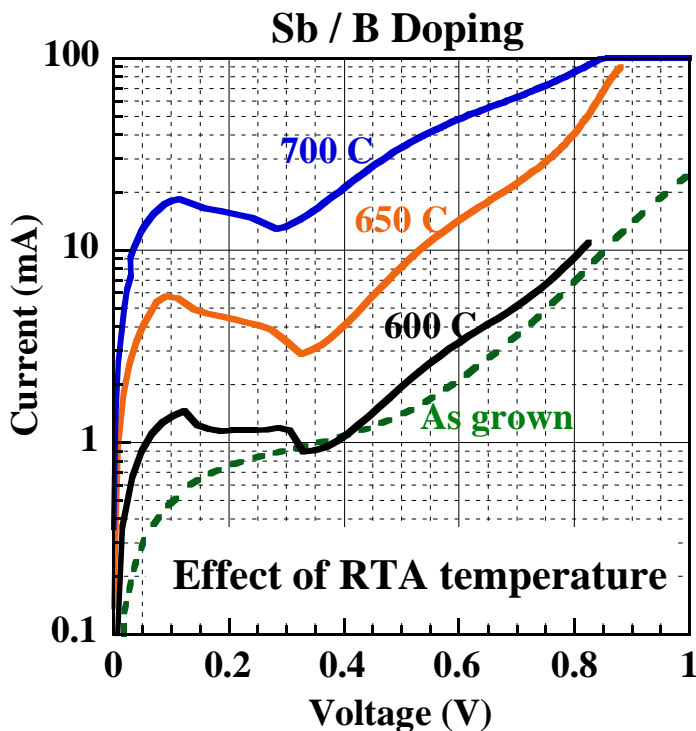
Tunnel junction before and after RTA and calculated peak current (inset) [1].

[1] P. Thompson et al., Appl. Phys. Lett., **75**, 1308 (1999)

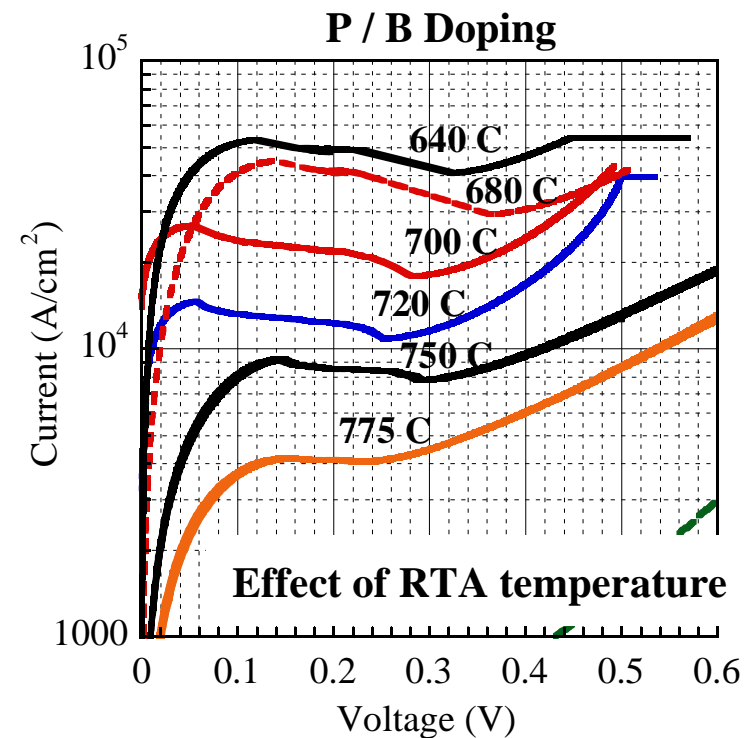
## Open Questions: Dopant Species

How do they affect device performance?

- Sb segregates but does not diffuse.
- Historically, PVCR was highest with Sb doping, second highest with As doping, and lowest with P doping for both Si and Ge tunnel diodes [1].
- Currently, the highest PVCR comes from P doped devices [2].



P. Thompson et al., Appl. Phys. Lett., **75**, 1308 (1999)



M. Dashiell et al., preprint.

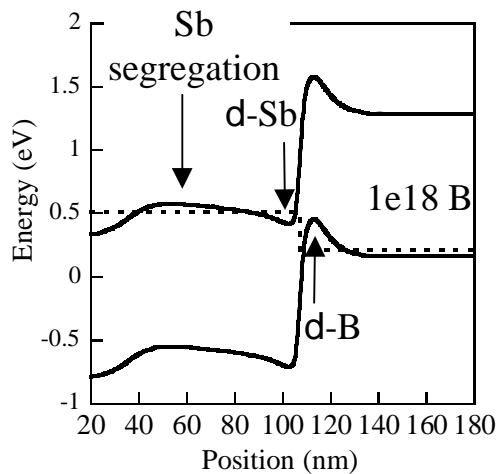
[1] R. A. Logan and A. G. Chynoweth, Phys. Rev., **131**, 89 (1963).

[2] R. Dushcl et al., Electronics Lett., **35**, 1111 (1999).

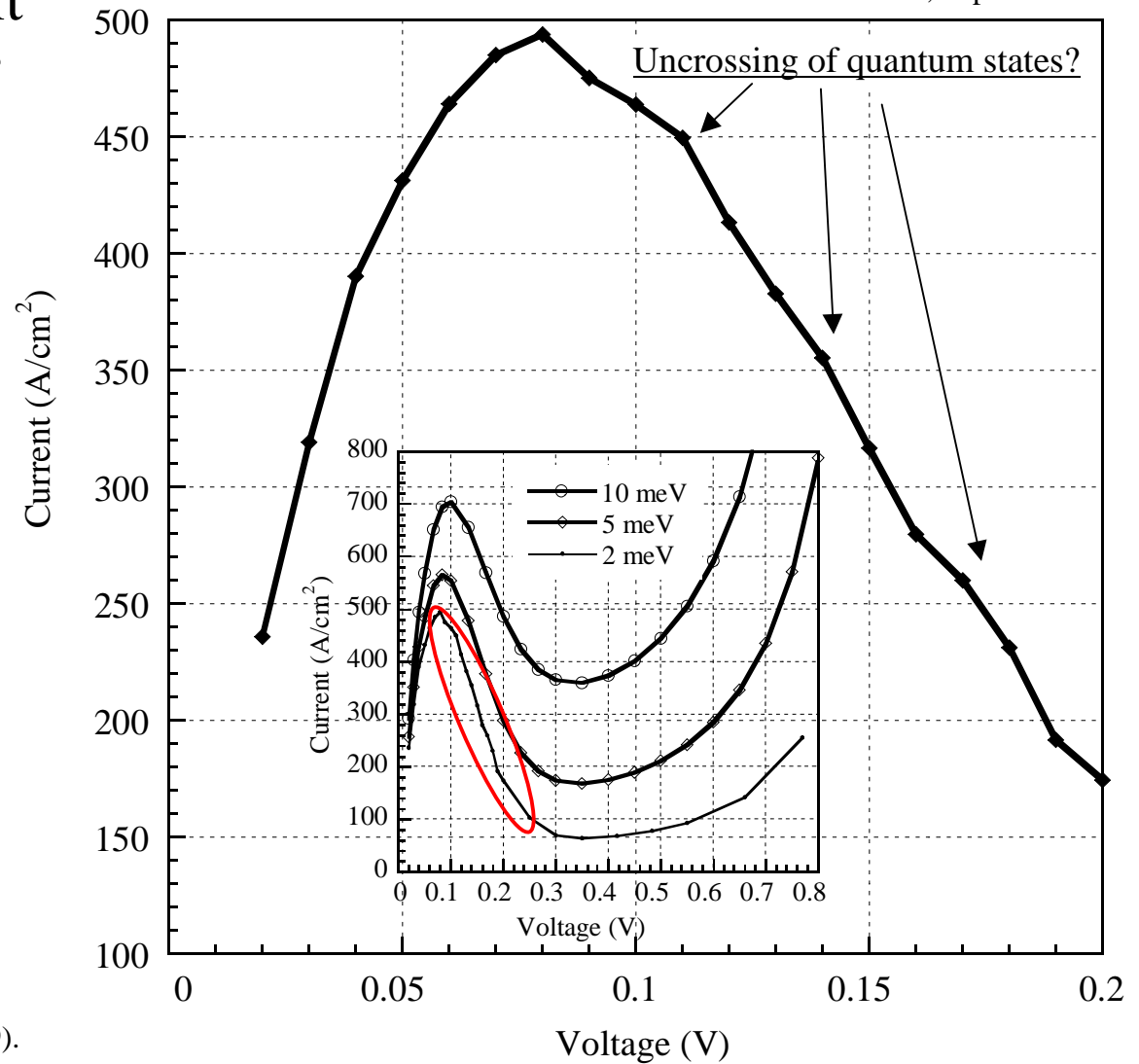
# Open Questions: Delta Doping

Is it necessary? How does it affect device performance?

- The highest PVCR has been observed in d-doped devices [1].
- The highest current density has been observed in non-delta doped device [2].
- What is the effect of the quantum states in the d-doped wells?



C. Rivas et al., unpublished.



[1] R. Dushcl et al., Electronics Lett., **35**, 1111 (1999).

[2] M. Dashiell et al., preprint.

## Open Questions: The x in the $\text{Si}_x\text{Ge}_{1-x}$

- Do we need  $\text{Si}_x\text{Ge}_{1-x}$ ?
  - For high current density, minimize x to minimize  $E_G$ .
  - BUT, the highest current density has been observed in an all-Si device [1].
- What is the optimum value of x?

[1] M. Dashiell et al., preprint.

## How About Carbon? SiGeC?

- Diffusion barrier?
- Offsets?
- Band Gaps?

## Forward Looking Issue - Scaling?

- How small in diameter can we make tunnel diodes?
  - Surface recombination will reduce PVCR.
- How small do we want to make them?
- For maximum speed -
  - Minimum area (minimum capacitance) maximum current density diodes.

## Conclusions

- First working design built 5/98 followed by rapid progress.
- Published PVCR of 4.2.
- Published current densities of 22 kA/cm<sup>2</sup>.
- Speed index - maximize current density ==> minimize intrinsic layer length.
  - Maximum estimated of 30 V GHz.
- PVCR - maintain clean intrinsic tunnel region.
  - Maximum of 4.2 published with better results already obtained.
- Nanometer control of dopant profiles is key to optimizing both speed index and PVCR.
  - Processing, dopant species, diffusion barriers.
- Open Questions: The x in Si<sub>x</sub>Ge<sub>1-x</sub>? Dopant species? d-doping? SiGeC?  
Scaling?