Digital Integrated Circuit (IC) Layout and Design - Week 3, Lecture 5

- http://www.ee.ucr.edu/~rlake/EE134.html

Reading and Prelab

- Week 1 - Read Chapter 1 of text.
- Week 2 - Read Chapter 2 of text.
- Week 3 - Read Chapter 3 of text.
- Prelab - Lab 1.
  - Read insert A of text, pp. 67 - 71.
  - The lab will make more sense if you read this before lab.
  - There is nothing to turn in.

Agenda

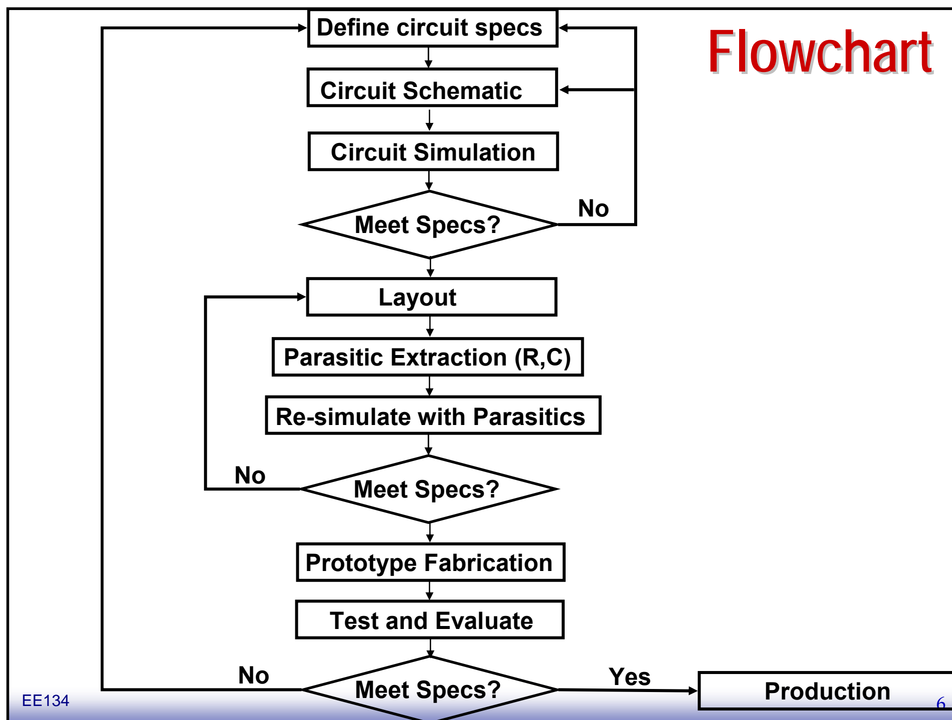
- Last Lecture
  - Design rules
  - Layout and Design
  - Ties to V_{DD} and GND
  - Padframes
  - Pin Packages
- Today's Lecture
  - Contacts
  - Basic MOS transistor operation
  - Large-signal MOS model for manual analysis
  - The CMOS inverter

Course Emphasis / Design Styles

- Physical design of CMOS digital ICs
- Application Specific IC (ASIC)
  - Full Custom (What we are doing)
    - Most flexible approach
    - Higher speed
    - Smaller designs
    - Expensive
    - Requires device-level (i.e. transistor level) knowledge
    - Push limits of a technology - must understand parasitics: stray C, L, pn jns., BJTs, breakdown, stored charge, latch-up, etc.
    - Used for high-volume chips - μ–processors & memory

Design Styles (cont.)

- ASIC (cont.)
  - **Standard Cell**
    - Logic gate level
    - Low volume
    - Quick turnaround
    - Lower density
  - **Gate Array (FPGA)**
    - Lowest density - speed - cost.



Tie n-well to VDD and Substrate to Ground

(a) Layout

Reason for GND and V_{DD} Ties

Parasitic Diodes

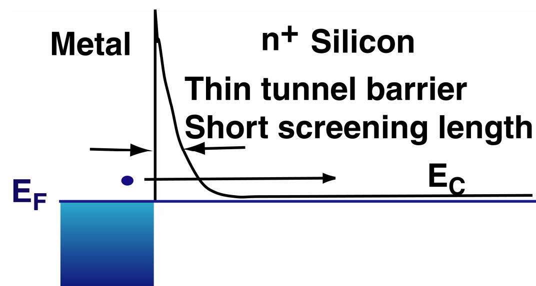
Contacts to Silicon

- **Ohmic Contacts**
  - **Metal on highly doped n^+ or p^+ Si.**
  - **What you want to pin the substrate to ground or the n-well to V_{DD}.**
- **Schottky Contacts (we won't use these)**
  - **Metal on lightly doped n or p Si.**
  - **Creates a Schottky diode which has an I-V curve similar to a p-n junction diode.**

EE134 9

Ohmic contact

- **Metal on n^+ or p^+ Si.**
- **Simple picture:**

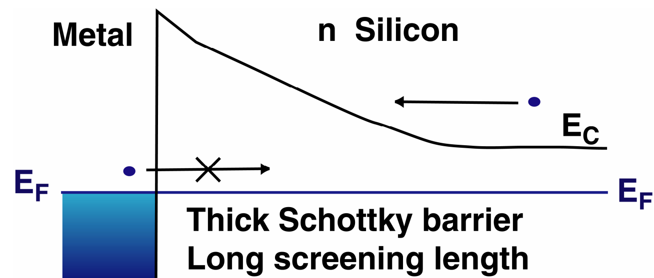


- **Need heavy doping to get the ultra short screening length needed for an OHMIC contact.**

EE134 10

Schottky Contact

- Metal on n or p Si.
- Simple picture:

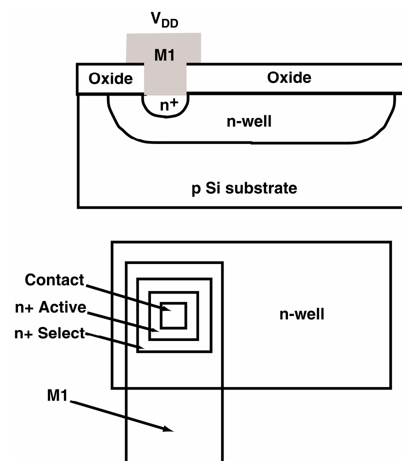


- Light n or p doping gives long screening length giving Schottky Barrier.

EE134 11

Ohmic Contacts for Voltage Pinning

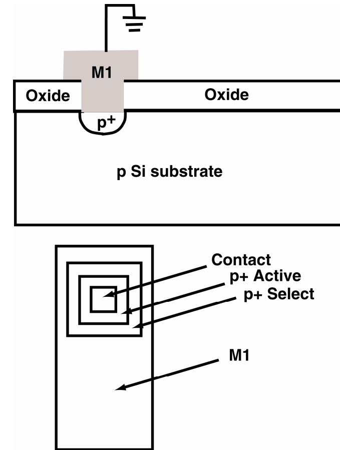
- Ohmic contact to the n-well
- You need the
  - Active and Select to define the n+ region.
  - Contact to put hole in thick passivation oxide / nitride so that the metal contacts the Si.



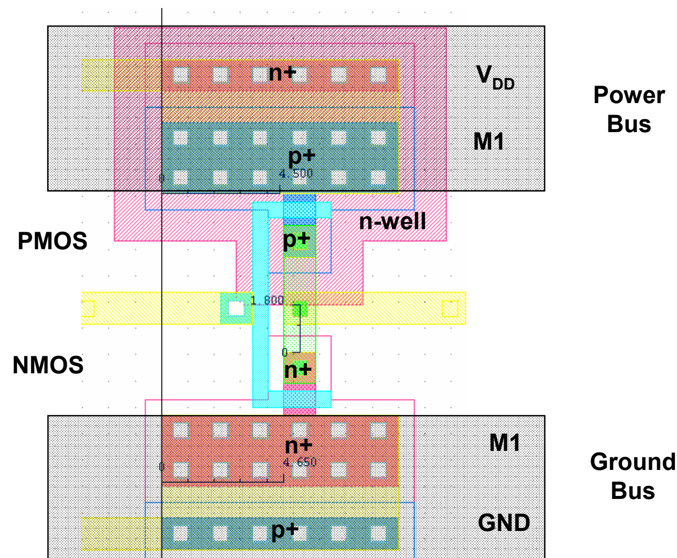
EE134 12

Ohmic Contacts for Voltage Pinning

- Ohmic contact to the p-substrate
- You need the
  - Active and Select to define the p+ region.
  - Contact to put hole in thick passivation oxide / nitride so that the metal contacts the Si.

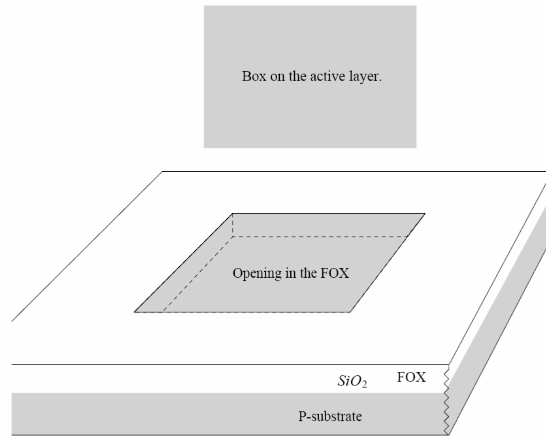


Pin n-well to V_{DD} and p-substrate to GND

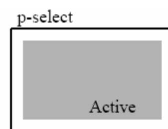


The Active Layer

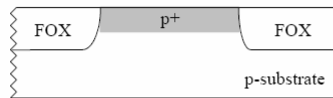
- Cut in the Field Oxide (FOX) to get down to the Si.



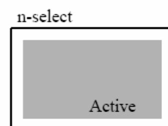
Active and Select Layers



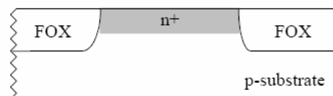
(a) Layout



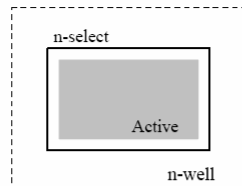
(b) Cross-sectional view for (a)



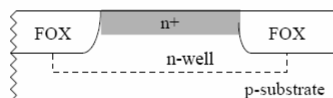
(c) Layout



(d) Cross-sectional view for (c)

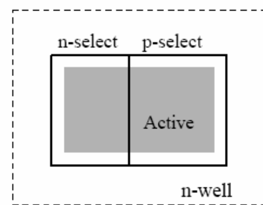


(e) Layout

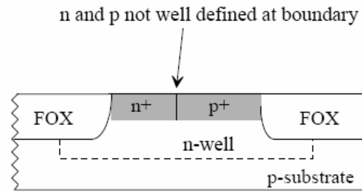


(f) Cross-sectional view for (g)

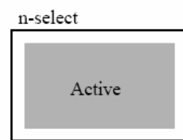
Active and Select Layers (cont)



(g) Layout

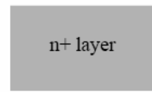


(h) Cross-sectional view for (g)



(i) two layers

Drawn as a single layer



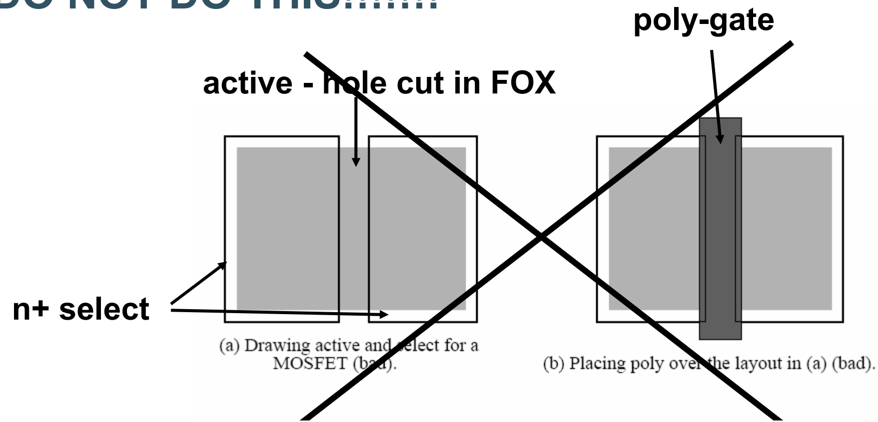
(j) Drawn as a single layer

4 Concepts to Remember:

- **Need to put down an n+ region on the n-well to make an ohmic contact to the n-well.**
- **Need to put down a p+ region on the p-substrate to make an ohmic contact to the p-substrate.**
- **These are your active / select layers.**
- **Finally, you need a contact layer to drill through the thick oxide / nitride passivation.**

BAD MOS Layout

❑ DO NOT DO THIS!!!!!!!



- **Self-aligned process**
  - **The Poly gate serves as an implant mask during the n+ implant.**
  - **There is no gap between the source/gate and drain/gate.**

Outline

Ch. 3

❑ **MOS Transistor**
- Basic Operation
- Modes of Operation
- Deep sub-micron MOS

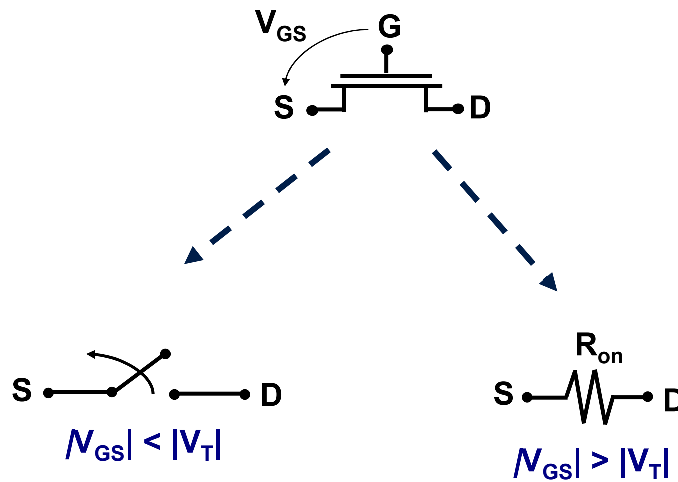
❑ **CMOS Inverter**

EE134 20

What is a Transistor?

An MOS Transistor ⟷ A Switch!

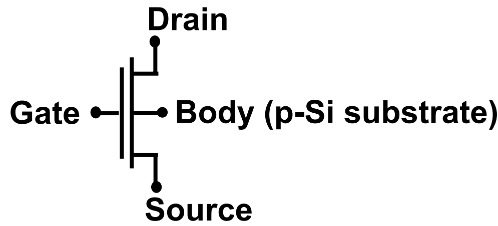
Switch Model of CMOS Transistor

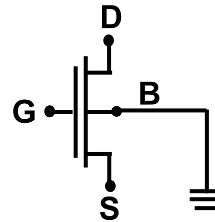


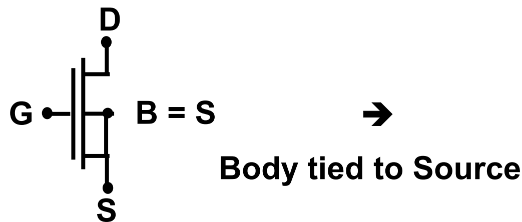
Transistor Circuit Symbols

❑ **NMOS**

We always want





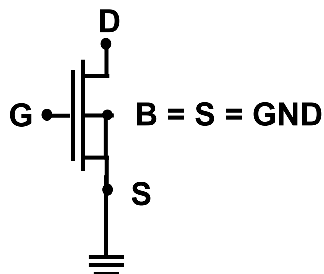


EE134 23

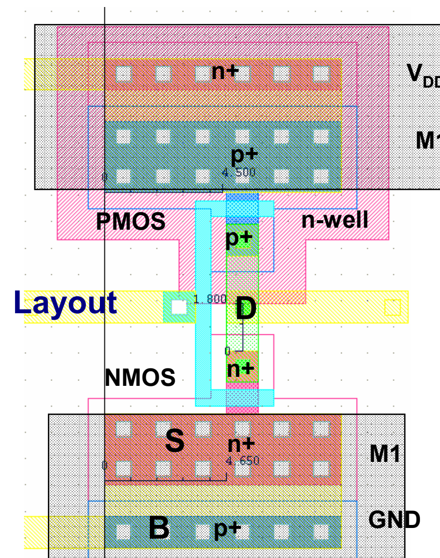
NMOS Body Terminal (B)

- **A transistor is a 4 terminal device.**

Circuit Schematic



Layout



EE134 24

Transistor Circuit Symbols

- PMOS

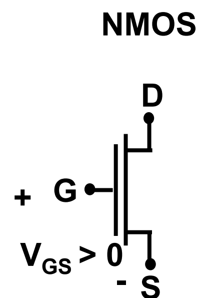
We always want

PMOS Body Terminal (B)

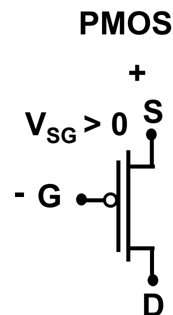
NMOS and PMOS

- PMOS is complementary to NMOS
- Turn it upside down and switch all signs of voltages, V_{SD} ➔ V_{DS}, V_{GS} ➔ V_{SG}.

NMOS



PMOS



EE134 27

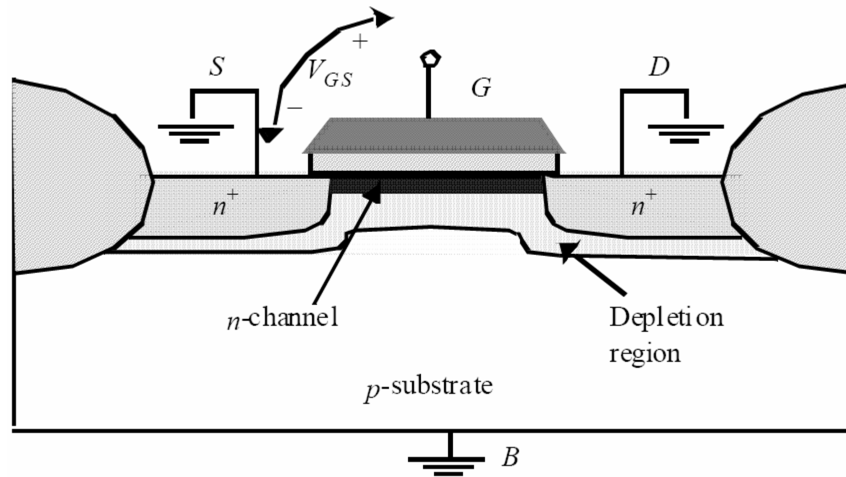
Outline

Ch. 3

- MOS Transistor
  - Basic Operation
  - **Modes of Operation**
  - **Deep sub-micron MOS**
- CMOS Inverter

EE134 28

Threshold Voltage: Concept



The Threshold Voltage

$$V_T = \phi_{ms} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

Workfunction Difference

Depletion Layer Charge

Surface Charge

Implants

Body Effect Coefficient

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

with

$$V_{T0} = \phi_{ms} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_I}{C_{ox}}$$

and

$$\gamma = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

Fermi Potential

$$\phi_F = -\phi_T \ln\left(\frac{N_A}{n_i}\right)$$

$$\phi_T = \frac{k_B T}{q}$$

$2\phi_F \approx$ -0.6V for p-type substrates

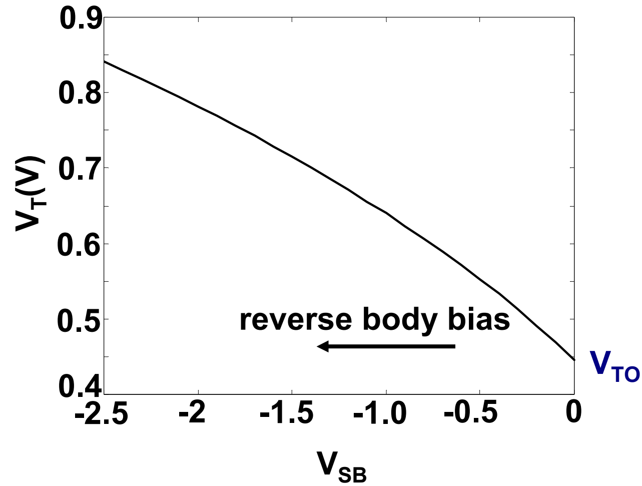
γ is the body factor

V_{T0} = 0.76 V (NMOS)

0.95 V (PMOS)

AMI C5 process

The Body Effect



The Drain Current

- **Charge in the channel is controlled by the gate voltage:**

$$Q_i(x) = -C_{ox}[V_{GS} - V(x) - V_T] \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- **Drain current is proportional to charge x velocity:**

$$I_D = -v_n(x) \cdot Q_i(x) \cdot W$$

$$v_n(x) = -\mu_n \cdot \xi(x) = \mu_n \frac{dV}{dx}$$

v_n = velocity; W = channel width; ξ = electric field; μ_n = mobility

The Drain Current

- Combining velocity and charge:

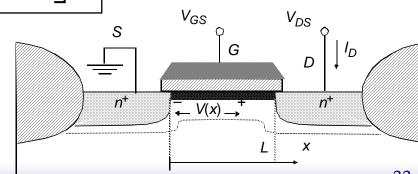
$$I_D \cdot dx = \mu_n \cdot C_{ox} \cdot W \cdot (V_{GS} - V - V_T) \cdot dV$$

- Integrating along the length of the channel from source to drain:

$$\int_0^{L_G} I_D \cdot dx = \int_0^{V_{DS}} \mu_n \cdot C_{ox} \cdot W \cdot (V_{GS} - V - V_T) \cdot dV$$

$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$k'_n = \mu_n \cdot C_{ox} = \frac{\mu_n \cdot \varepsilon_{ox}}{t_{ox}}$$



Outline

Ch. 3

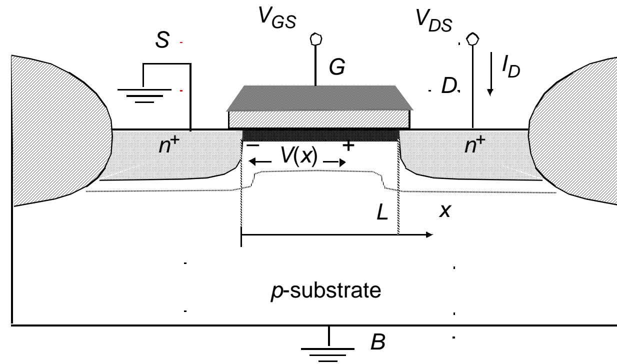
- MOS Transistor
  - **Basic Operation**
  - Modes of Operation
  - **Deep sub-micron MOS**
- CMOS Inverter

Transistor in Linear Mode

$V_{GS} > V_{DS} + V_T$

$V_{DS} < V_{GS} - V_T$

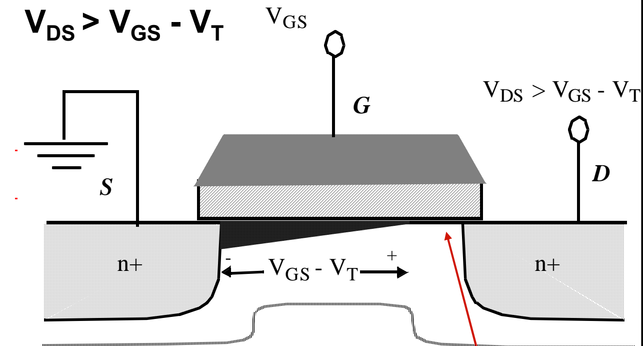
Device turned on ($V_{GS} > V_T$)



$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Transistor in Saturation

$V_T < V_{GS} < V_{DS} + V_T$ $\quad V_{DS} > V_{GS} - V_T$



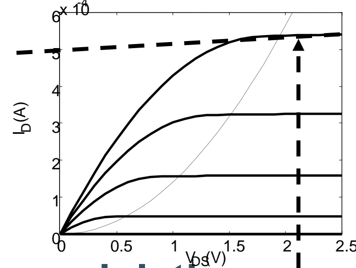
$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

Saturation

- For $V_{DS} > V_{GS} - V_T$, the drain current saturates:

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$



- Including channel-length modulation:

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS})$$

slope = λV_{DS}
= V_{DS}/V_A

$V_A = 1/\lambda$ = Early voltage

Modes of Operation

- Cutoff:

$V_{GS} < V_T$ $\quad$ $I_D = 0$

- Resistive or Linear:

$V_{DS} < V_{GS} - V_T$ &
$V_{GS} > V_T$

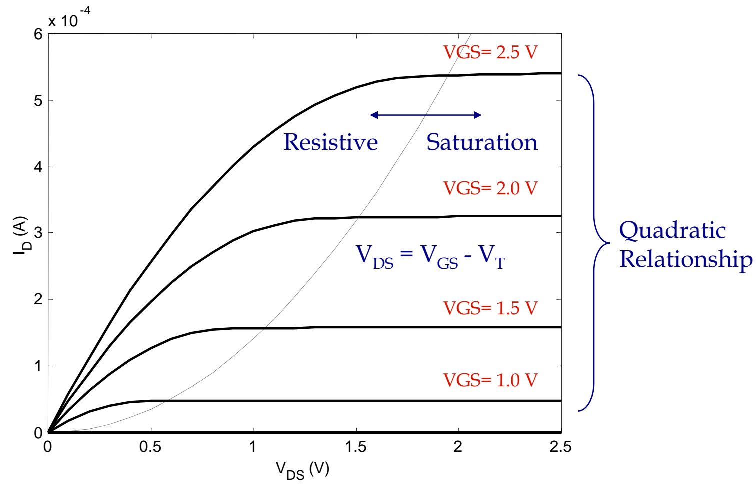
$$I_D = \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

- Saturation

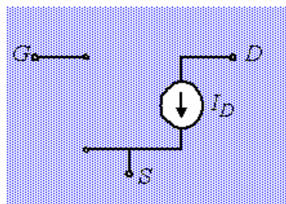
$V_{DS} > V_{GS} - V_T$
$V_{GS} > V_T$

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

Current-Voltage Relations
A good ol' Transistor



A model for manual analysis



$V_{DS} > V_{GS} - V_T$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

$V_{DS} < V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right)$$

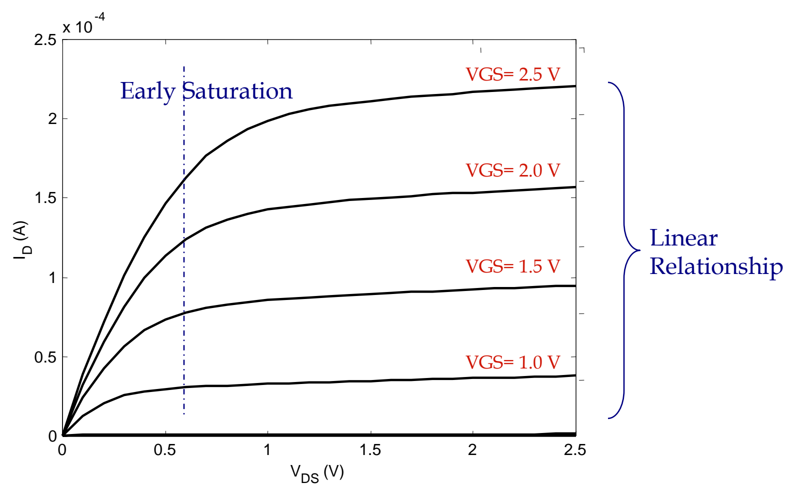
Outline

Ch. 3

- ❑ **MOS Transistor**
  - **Basic Operation**
  - **Modes of Operation**
  - Deep sub-micron MOS
- ❑ **CMOS Inverter**

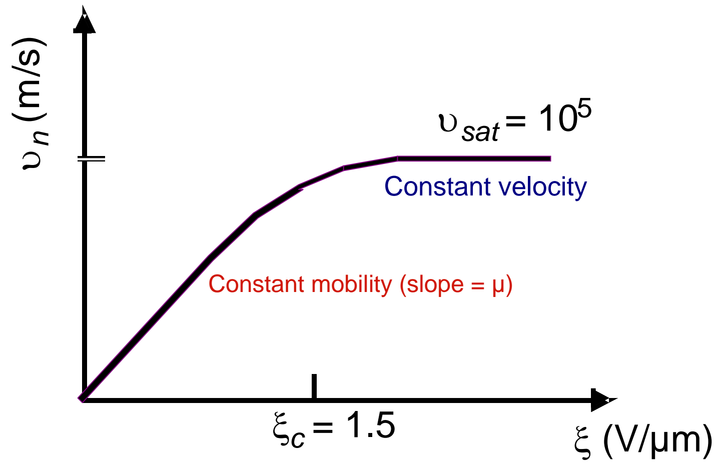
EE134 41

Current-Voltage Relations The Deep-Submicron Era

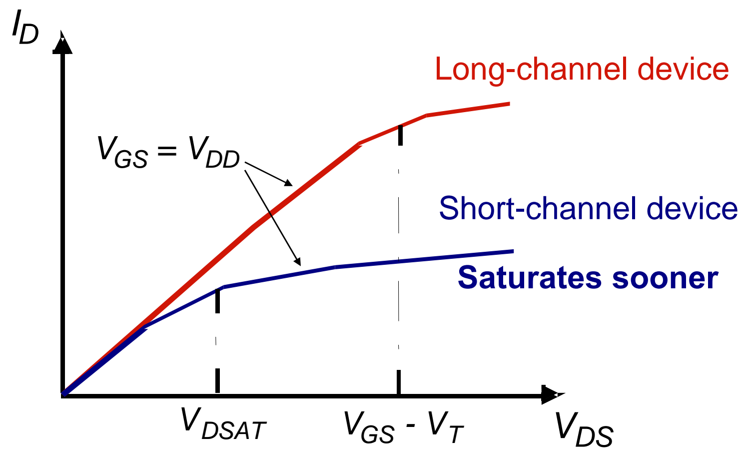


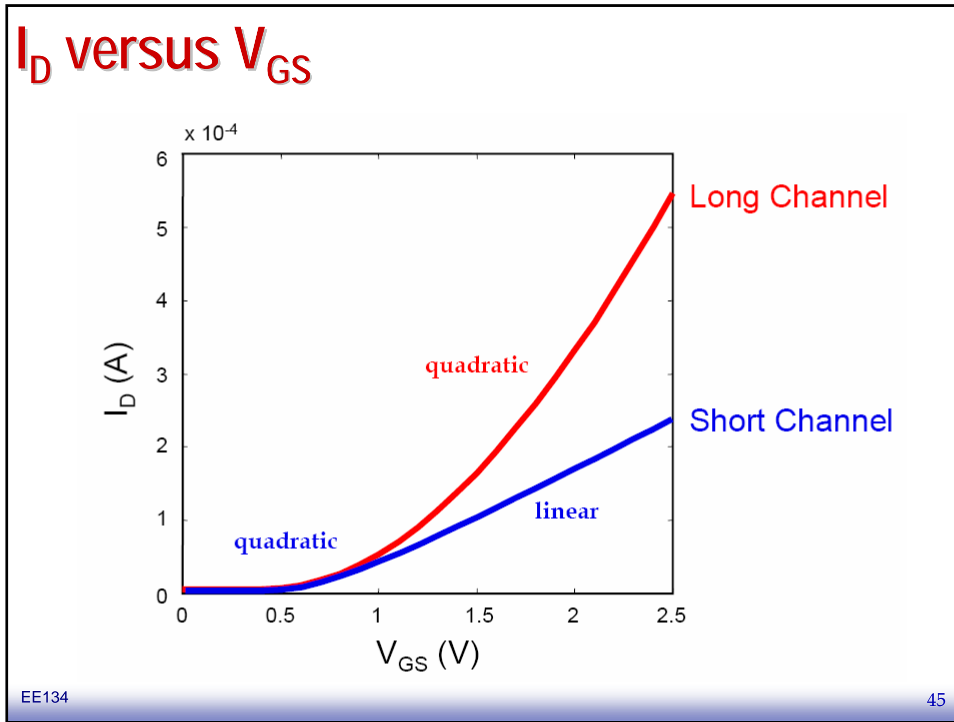
EE134 42

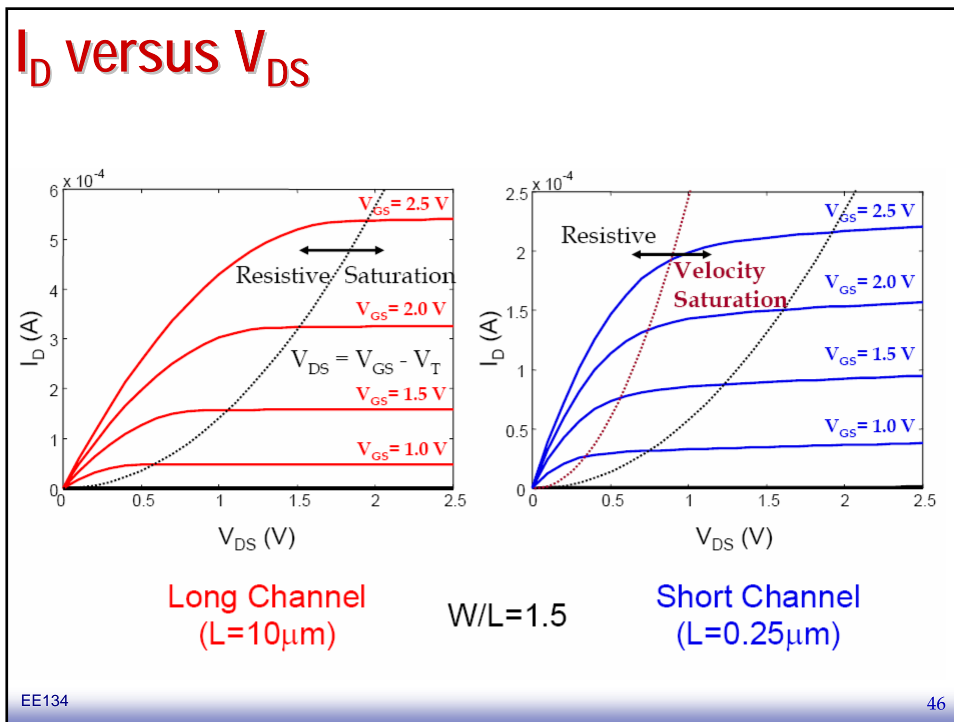
Velocity Saturation



Velocity Saturation




I_D versus V_GS
x 10^-4
6
5
4
3
2
1
0
I_D (A)
0
0.5
1
1.5
2
2.5
V_GS (V)
Long Channel
quadratic
Short Channel
linear
quadratic
EE134
45


I_D versus V_DS
x 10^-4
V_GS = 2.5 V
Resistive
Saturation
V_GS = 2.0 V
V_DS = V_GS - V_T
V_GS = 1.5 V
V_GS = 1.0 V
I_D (A)
V_DS (V)
Resistive
Velocity
Saturation
V_GS = 2.5 V
V_GS = 2.0 V
V_GS = 1.5 V
V_GS = 1.0 V
Long Channel
(L=10μm)
W/L=1.5
Short Channel
(L=0.25μm)
EE134
46

Including Velocity Saturation

- Approximate velocity:

$$\upsilon = \frac{\mu_n \cdot \xi}{1 + \xi / \xi_c} \qquad \text{for } \xi \le \xi_c$$

$$\upsilon = \upsilon_{sat} \qquad \text{for } \xi \ge \xi_c$$

μ_n chosen empirically so that $\frac{\mu_n \xi_c}{2} = v_{sat}$

➔ μ_n depends on the SPICE model.

- And integrate current again:

$$I_D = \frac{\mu_n \cdot C_{ox}}{1 + (V_{DS} / \xi_c \cdot L)} \cdot \frac{W}{L} \cdot \left[(V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$

n **deep submicron**, there are four regions of operation:
1) cutoff, (2) resistive, (3) saturation and (4) **velocity saturation**

Simple Cheesy Derivation for Velocity Saturation and Linear Dependence on V_{GS}

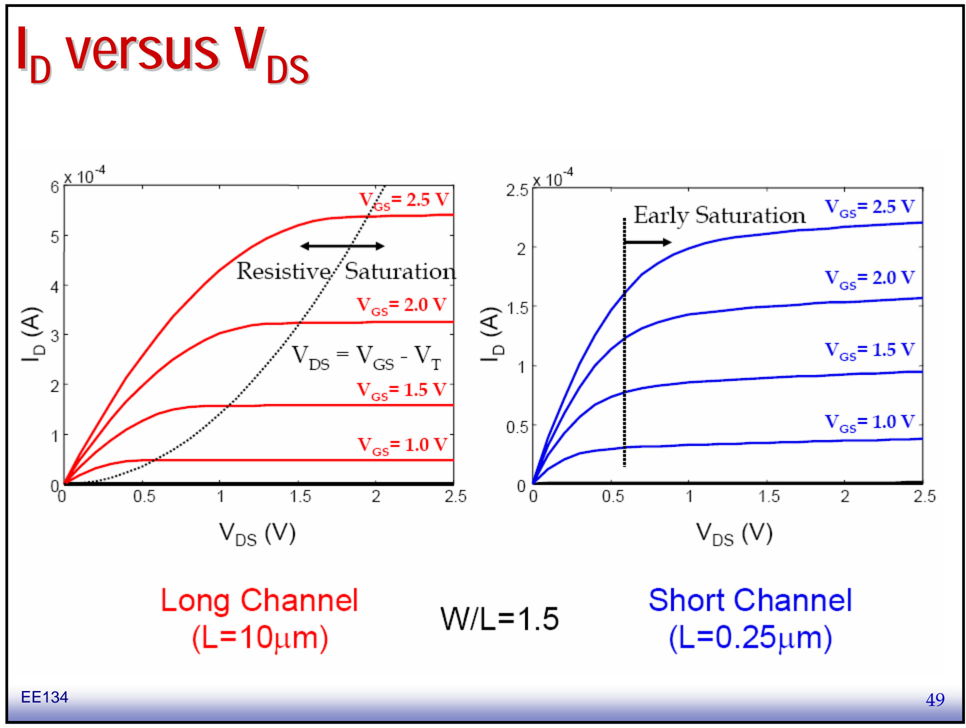
$$I_D = W \underbrace{\mu_n \frac{dV}{dx}}_{\text{velocity}} \underbrace{C'_{ox}(V_{GS} - V_{TH} - V(x))}_{\rho_{2D}\text{ (charge density)}}$$

$$I_D = W\, v\, \rho_{2D}$$

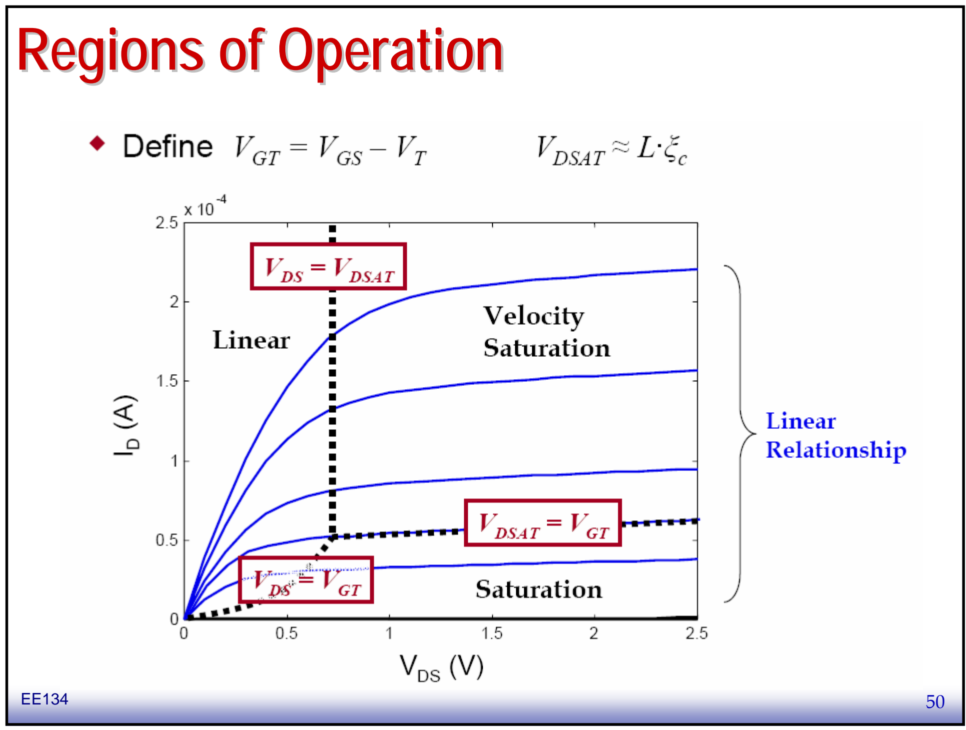
By definition, $\mu_n \equiv \frac{v}{\xi} = \frac{v}{dV/dx}$

$$I_D = W \frac{v_{sat}}{dV/dx} \frac{dV}{dx} C'_{ox}(V_{GS} - V_{TH} - V_{DS,sat})$$

$$I_D = W\, v_{sat}\, C'_{ox}(V_{GS} - V_{TH} - V_{DS,sat})$$

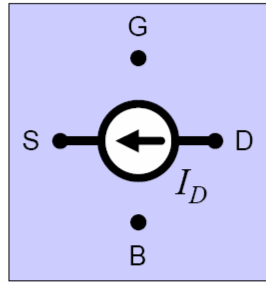


I_D versus V_DS
x 10^-4
V_GS = 2.5 V
Resistive
Saturation
V_GS = 2.0 V
V_DS = V_GS - V_T
V_GS = 1.5 V
V_GS = 1.0 V
I_D (A)
V_DS (V)
Early Saturation
Long Channel
(L=10μm)
W/L=1.5
Short Channel
(L=0.25μm)
EE134
49



Regions of Operation
Define $V_{GT} = V_{GS} - V_T$ $V_{DSAT} \approx L \cdot \xi_c$
x 10^-4
$V_{DS} = V_{DSAT}$
Linear
Velocity Saturation
Linear Relationship
$V_{DSAT} = V_{GT}$
$V_{DS} = V_{GT}$
Saturation
I_D (A)
V_DS (V)
EE134
50

A Unified Model for Manual Analysis



define $V_{GT} = V_{GS} - V_T$

for $V_{GT} \leq 0$: $I_D = 0$

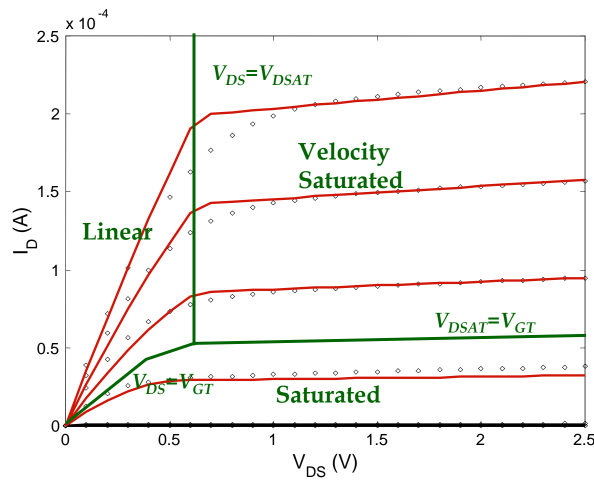
for $V_{GT} \geq 0$:

$$I_D = k' \cdot \frac{W}{L} \cdot \left(V_{GT} \cdot V_{\min} - \frac{V_{\min}^2}{2} \right) \cdot (1 + \lambda \cdot V_{DS})$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$

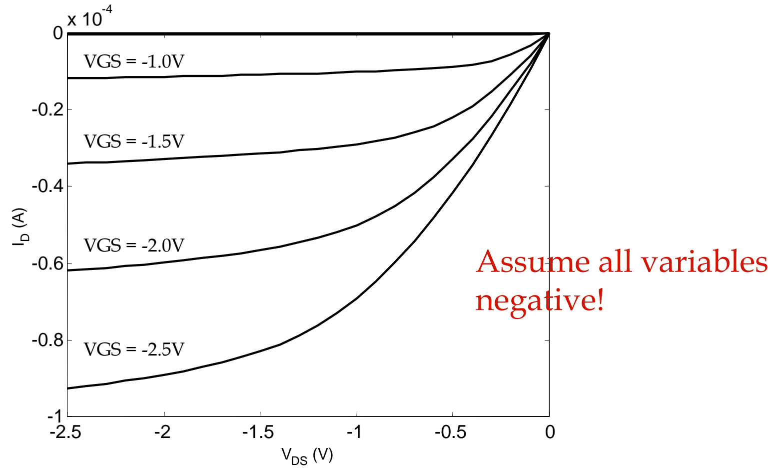
EE134 51

Simple Model versus SPICE



EE134 52

A PMOS Transistor

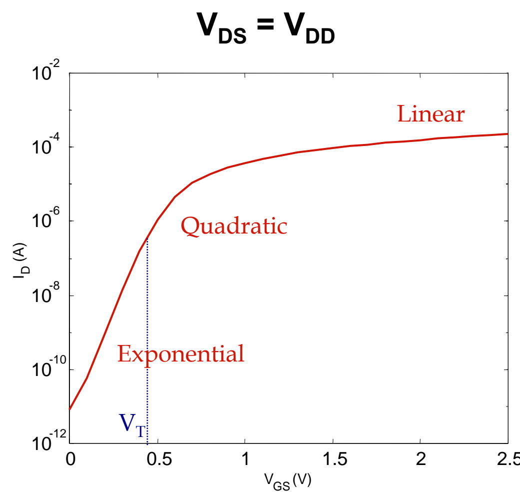


Assume all variables negative!

EE134 53

Sub-Threshold Conduction (Cut-off)

$V_{DS} = V_{DD}$



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S: 60 .. 100 mV/decade

S = inverse subtheshold slope

EE134 54

Subthreshold

- Inverse sub-threshold slope (S)
  - Ideal value @ T=300K, n=1,

$$S = \frac{k_B T}{q}\ln(10) = 60\,\frac{\text{mV}}{\text{decade}}$$

  - For each 60 mV of V_{GS}, the current drops by a factor of 10. This is the best that you can do.
  - For V_{DD} = 0.4V, the maximum on-off current ratio that you can have at T=300K is

$$10^{\frac{400}{60}} = \boxed{4.6\times10^{6}}$$

  - At 373K, the ratio is

$$10^{\frac{400}{74}} = \boxed{2.3\times10^{5}}$$

Subthreshold

- Current in subthreshold

$$I_D = I_S e^{\frac{V_{GS}}{nk_BT/q}}\left(1 - e^{-\frac{V_{DS}}{k_BT/q}}\right)(1+\lambda V_{DS})$$

- Inverse subthreshold slope definition

$$S \equiv \left(\frac{d(\log_{10} I_{DS})}{dV_{GS}}\right)^{-1} = \left(\frac{1}{\ln 10}\,\frac{1}{I_{DS}}\,\frac{dI_{DS}}{dV_{GS}}\right)^{-1}$$

$$S = \frac{nk_BT}{q}\ln 10$$

Subthreshold Concepts

- FETs turn off exponentially.
- Inverse subthreshold slope, S (mV/dec), is the figure of merit that tells how well they shut off. $S = \frac{nk_BT}{q}\ln(10) \underset{n=1}{=} \begin{cases} 60\ \text{mV/dec @ } 27^{o}\text{C} \\ 74\ \text{mV/dec @ } 100^{o}\text{C} \end{cases}$

  $n \geq 1$ and typically ≈ 1.5
- The maximum possible on-off current ratio is $\frac{I_{on}}{I_{off}}|_{max} = 10^{V_{DD}/S}$
- 2018 ITRS node has V_{DD} = 0.4V - hence the static power problem.

Know this if you are in an interview with a semiconductor co.

Transistor Model for Manual Analysis

Table 3.2 Parameters for manual model of generic 0.25 μm CMOS process (minimum length device).

	V_{T0} (V)	γ ($V^{0.5}$)	V_{DSAT} (V)	k' (A/V^2)	λ (V^{-1})
NMOS	0.43	0.4	0.63	115×10^{-6}	0.06
PMOS	−0.4	-0.4	-1	-30×10^{-6}	-0.1

EE134 58