Digital Integrated Circuit (IC) Layout and Design

- EE 134 – Winter 05
  - Lecture Tu & Thurs. 9:40 – 11am ENGR2 142
  - 2 Lab sections
    - M 2:10pm – 5pm ENGR2 128
    - F 11:10am – 2pm ENGR2 128
  - NO LAB THIS WEEK
  - FIRST LAB Friday Jan. 20

People

- Lecturer - Roger Lake
  - Office – ENGR2 Rm. 437
  - Office hours - MW 4-5pm
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- TA – Faruk Yilmaz
  - Office – ENGR2 Rm. 222
  - Office Hours – TBD
  - faruk@ee.ucr.edu
EE134 Web-site

- [http://www.ee.ucr.edu/~rlake/EE134.html](http://www.ee.ucr.edu/~rlake/EE134.html)
  - Class lecture notes
  - Assignments and solutions
  - Lab and project information
  - Exams and solutions
  - Other useful links

Class Organization

- **Homework assignments (10%)**
- **Labs (20%)**
  - Tutorials to learn the Cadence design software
- **Final Project (50%)**
  - Design a digital circuit (eg. 4 bit adder)
  - Work in teams of 3
- **Midterm (20%)**
Text Book

Digital Integrated Circuits: A Design Perspective, 2nd Ed.

Jan M. Rabaey
Anantha Chandrakasan
Borivoje Nikolic

Software

- Cadence software
  - Online documentation and tutorials
  - Sun4 UNIX Workstations
What is this book all about?

- Introduction to digital integrated circuits.
  - CMOS devices and manufacturing technology.
  - CMOS inverters and gates.
  - Propagation delay,
  - noise margins, and
  - power dissipation.
  - Sequential circuits. Arithmetic, interconnect, and memories.

- What will you learn?
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: cost, speed, power dissipation, and reliability

Digital Integrated Circuits

- Introduction: Issues in digital design
- CMOS devices and manufacturing
- The CMOS inverter
- Combinational logic structures
- Propagation delay, noise margins, power
- Sequential logic gates; timing
- Interconnect: R, L and C
- Arithmetic building blocks
- Memories and array structures
- Design methods
Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?
The First Computer (1832)

The Babbage Difference Engine (1832)
25,000 parts
cost: £17,470

ENIAC - The first electronic computer (1946)
The Transistor Revolution

First transistor
Bell Labs, 1948

The First Integrated Circuits

Bipolar logic
1960’s

ECL 3-input Gate
Motorola 1966
Intel 4004 Micro-Processor (1971)

1971
2,300 transistors
108 KHz operation

Intel Pentium 4 microprocessor (2000)

42 M transistors (217 mm²)
1.5 GHz
0.18 µm
180 nm technology node
What Happened over 30 Years?

1971

2,300 transistors
108 KHz operation

2000

42 M transistors
1.5 GHz operation

~ 15,000 x

Automotive comparison: SF to NY in 13 seconds.

Moore’s Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.

- He made a prediction that semiconductor technology will double its effectiveness every 18 months
Moore’s Law

Electronics, April 19, 1965.

Evolution in Complexity
Transistor Counts

1 Billion Transistors

Source: Intel

Moore’s law in Microprocessors

2X growth in 1.96 years!

Transistors on Lead Microprocessors double every 2 years

Courtesy, Intel
Die Size Growth

Die size grows by 14% to satisfy Moore’s Law

Frequency

Lead Microprocessors frequency doubles every 2 years

Doubles every 2 years
Power Dissipation

Lead Microprocessors power continues to increase

Power will be a major problem

Power delivery and dissipation will be prohibitive
**Power density**

![Graph showing power density over time](image)

Power density too high to keep junctions at low temp

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**Not Only Microprocessors**

Cell Phone

Digital Cellular Market (Phones Shipped)

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<tbody>
<tr>
<td>Units (M)</td>
<td>48</td>
<td>162</td>
<td>435</td>
<td>513</td>
<td>648</td>
<td>(703)</td>
<td>(776)</td>
<td>(836)</td>
<td>(889)</td>
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Challenges in Digital Design

∞ (# Transistors)
∞ 1/(Transistor size)

“Microscopic Problems”
• Ultra-high speed design
• Interconnect
• Noise, Crosstalk
• Reliability, Manufacturability
• Power Dissipation
• Clock distribution.

“Macroscopic Issues”
• Time-to-Market
• Millions of Gates
• High-Level Abstractions
• Reuse & IP: Portability
• Predictability
• etc.

Everything Looks a Little Different

...and There’s a Lot of Them!

Productivity Trends

Complexity outpaces design productivity

Source: Sematech

Courtesy, ITRS Roadmap
Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels

![Diagram showing design abstraction levels from system to device](image)
Next Class

- Introduce basic metrics for design of integrated circuits – how to measure delay, power, etc.

- Introduction to IC manufacturing and design.