EE134 Midterm W06

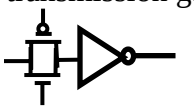
1. Sizing a chain of inverters to drive a large capacitive load:
A minimum size inverter has W/L = 0.375 / 0.25 for both the NMOS and PMOS using the example process of the text. A signal from this inverter must drive a 20pF output pin with a delay time, t_p, of less than 3ns. Design an inverter chain with a minimum number of inverters to meet this specification. Do not assume that $\gamma = 1$. Use capacitance and resistance values from the solution to problem 1 of HW 3.
a. Calculate the average value of C_{int}.
b. Calculate γ.
c. Calculate t_{p0}.
d. Determine the number of inverters N.
e. What are the gate widths of each inverter in the chain?

2. Static CMOS AOI logic:
a. Draw the transistor implementation of a 3 input NAND gate.
b. Draw the transistor implementation of a 3 input NOR gate.
c. Explain why one gate is preferable to the other in this logic style.

3. Design a static CMOS AOI logic gate:
a. Draw the static CMOS (AOI) implementation of $Y = \overline{A(B+CD) +E}$ such that capacitance is minimized at the output.
b. Calculate the worst case pull up and pull down times for all minimum size transistors (W/L = 0.375 / 0.25) assuming a 50 fF load and ignoring all other capacitances.

4. Design and compare static CMOS AOI logic versus transmission gate logic:
An XOR gate can be constructed using static CMOS (AOI) logic or transmission gates. Assuming complements of all variables are available,
a. Draw the static CMOS (AOI) transistor implementation.
b. Draw the transmission gate transistor implementation.
c. Assume a 50fF load capacitance and ignore all other capacitances. Use all minimum size transistors (W/L = 0.375 / 0.25) using the example process of the text. Calculate the worst case delay time for each implementation.

5. Transmission gate latch:
Draw a transmission gate implementation of a positive latch, i.e. Q = D when CLK = 1 and Q latched when CLK = 0. Draw the transmission gates at the transistor level and use the inverter symbol for the inverters, i.e.



6. Transmission gate register:
a. Draw a transmission gate implementation of a negative edge-triggered register.
b. Fill in the timing diagram below.

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