

Transistors and Tunnel Diodes

For Analog/Mixed-Signal Circuits and Embedded Memory

(Invited)

A. Seabaugh, X. Deng[†], T. Blake[†], B. Brar, T. Broekaert, R. Lake, F. Morris, and G. FrazierRaytheon Systems Company, [†]Texas Instruments Incorporated
Dallas, TX 75243**Abstract**

An integrated tunnel diode/transistor process can be used to increase the speed of signal processing circuitry or reduce power at the same speed; in memory applications, tunnel diodes can be used to reduce static power dissipation ($>20\times$ in Si, $>1000\times$ in III-V materials) relative to conventional approaches. This paper summarizes recent progress in InP and Si-based tunnel diodes¹ and circuits.

Introduction

Integrated circuit (IC) performance is limited by the finite gain-bandwidth product of the transistor technology. By adding a high speed tunnel diode (TD) to an existing transistor process, circuit speeds and power scaling can typically be improved. This is due to the high speed of the TD compared to the transistor, and the reduced component count of the TD/transistor circuit compared to the transistor circuit.

While Si TD/transistor technology was explored extensively in the 1960s and 70s, it suffered from being fundamentally discrete; the early “demise of the tunnel diode was signaled by the arrival in force of the integrated circuit” (1). Today, with the precise growth control of molecular beam epitaxy (MBE) the impediments to adding tunnel diodes to transistor processes are largely removed and large-scale TD/transistor ICs are being developed for the first time (2-4).

In this paper we show that the TD, in particular the resonant tunneling diode (RTD), can be produced with high uniformity and good reproducibility. RTDs been combined with the InP-based HEMT (high electron mobility transistor) in a high speed large scale integration (LSI) process to produce gigahertz clocked circuits (2,3) and recent progress in this technology will be summarized. The focus of this paper however will be to revisit the Si TD/transistor prospects, particularly the addition of the TD with CMOS. For this we use SPICE simulation, based on Texas Instruments’ (TI) 0.25 μm CMOS models and an InP RTD model, fit to both dc and S-parameter measurements (4).

InP-Based RTD/HEMT Technology

The record highest speed transistors (HEMT), and TDs, (specifically, RTDs) have both been achieved on InP substrates with a cut-off frequency of 340 GHz (5) and switching speed of 1.5 ps (6) respectively. These devices have been combined with capacitors, resistors, and Schottky diodes in a monolithic IC format for gigahertz analog/mixed signal circuits and used to demonstrate: 4-bit, 3 GHz analog-to-digital converters (4), 3 GHz (50 dB spur free dynamic range) clocked quantizers (4), 3 GHz sample & hold circuits (55 dB linearity) (4), 5 GHz clock circuits (3), 2.5 GHz shift registers (3), and ultralow power SRAM (50 nW/bit) (7). Test equipment has limited the speeds at which these circuits could be characterized; clock rates in the range 10-100 GHz are projected from SPICE simulations.

These circuit demonstrations are made possible by the high uniformity of the MBE-grown RTD. This uniformity is shown in Fig. 1(a) where the current-voltage (I-V) characteristic of nine diodes are shown which span a 50 mm InP wafer. The dashed curves corresponding to the two outer RTD cells, closest to the wafer edge, while the solid lines are for the interior cells.

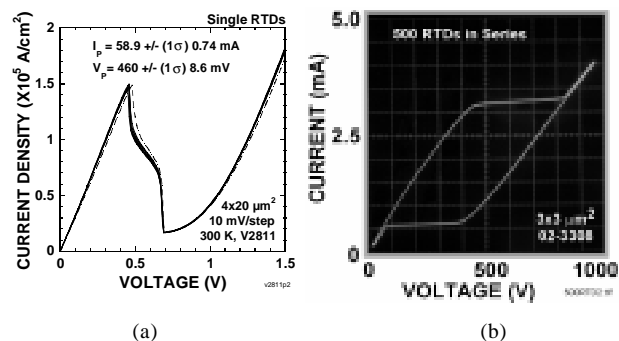


Fig. 1: Resonant tunneling diodes (RTDs): (a) position dependence of current-voltage characteristic across a 50 mm InP wafer (the edge devices are indicated by a dashed line) and (b) five hundred series-connected InP-based RTDs showing $\sim 3\%$ variation of peak and valley currents over the array. Both diodes use AlAs/InGaAsInAs/InGaAs/AlAs heterostructures.

¹ In this paper, “tunnel diode” refers broadly to p^+n^+ Esaki diodes and RTDs.

The RTD I-V characteristic is essentially determined by its layer dimensions, which set the diode peak current and peak voltage. Just as the turn-on voltage of a *p-n* diode is determined by the bandgap which is derived from the lattice spacing, the RTD critical parameters are also determined by bandgaps and lattice spacings. By MBE, thicknesses and compositions can be controlled precisely and uniformly as shown in Fig. 1 (a); even for an RTD with a peak current density exceeding 10^5 A/cm² (corresponding to a tunnel barrier thickness of approximately 6 monolayers) this layer dimension and the peak current are held essentially constant across the wafer.

Excellent local uniformity is shown in Fig. 1(b), a measurement of 500 RTDs connected in series. As the voltage is increased each of the 500 RTDs switches independently and in order from the lowest RTD peak current to the highest peak current. In this way the peak current of all 500 devices is sampled in a single measurement. On the return trace the switching order proceeds from the highest valley current to the lowest valley current and the valley current of all the devices is then also measured. From Fig. 1(b), the uniformity of peak and valley currents, which includes both material and process variations, can be seen to be less than ~3% in 500 devices.

Reproducibility is also under good control using MBE. Shown in Fig. 2 are measurements from two wafers which were grown consecutively then processed separately. The RTD peak current is plotted against device area showing that I-V characteristics have good run-to-run reproducibility in both growth and process.

CMOS/TD Circuits

A. Memory Cells

Tunnel diode growth on silicon is relatively immature. Recently however, CMOS-compatible interband tunnel diodes

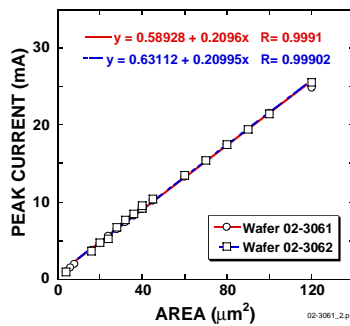


Fig. 2: Reproducibility of two separately grown and processed InP resonant tunneling diode wafers showing reproducibility and linearity of the diode formation process.

have been demonstrated (8,9) and show that a wide range of current-densities can be obtained spanning the range from 10^{-6} A/cm² (8) as required for embedded memory (10) to more than 20 kA/cm² (9) as needed for signal processing.

Dynamic random access memory (DRAM) cells have one access transistor and one capacitor in an integrated, highly specialized structure optimized for maximum density and minimum standby power. A process for embedding DRAM and logic on the same chip is desirable, but the periodic refreshing required for maintaining DRAM data adds complexity and consumes most of the DRAM power. A single-transistor (1T)/two-TD memory cell uses a DRAM cell topology, but with the addition of TDs eliminates the need for refreshing, and changes the cell storage from dynamic to static (SRAM) (7,10).

The tunnel SRAM cell is shown Fig. 3(a) where the currents I_3 , I_2 , and I_1 respectively represent the total leakage current through the access transistor and storage capacitor, the current through TD2, and the current through TD1. The leakage current versus node voltage and the I-V characteristics of the TDs are shown in Fig. 3(b). As shown in the same figure, the combined drive (I_2+I_3) and load (I_1) lines have two stable points, one near 1 V and the other near GND. It can be seen that the leakage current I_3 is completely compensated by the current difference I_1-I_2 , thereby storing the logic level statically. (Note the TDs do not drive the bit line; data readout is DRAM-like using sense amplifiers).

In Table 1, using TI's 0.25 μ m, 1.8 V, 0.7 μ m metal pitch, CMOS logic-process models, the TD SRAM is compared against DRAM and SRAM in terms of layout area, relative areas, and estimated read/write cycle time and standby currents. The cases which were examined are, in order of Table 1: a 6T SRAM, a DRAM cell with a gate oxide capacitor (C_g), the TD SRAM (Fig. 3a) with C_g , a DRAM cell with a stacked-capacitor (C_{st}) cell instead of C_g , and the TD SRAM with C_{st} .

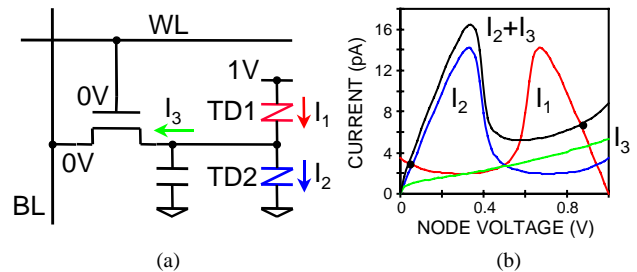


Fig. 3: CMOS/TD SRAM cell: (a) schematic diagram and (b) current-voltage relations.

TABLE 1
COMPARISON OF CMOS/TD SRAM CELLS WITH CMOS
EMBEDDED DRAM AND 6T SRAM

Process	Cell	Area (μm^2)	Density Ratio (x6T)	Cycle Time (ns)	Standby Current (pA)
CMOS	6T SRAM	7.00	1.0	4	7
CMOS	1T+1Cg DRAM	5.79	1.2	18	31
CMOS +TD	1T+1Cg+2TD SRAM	7.02	1.0	18	3
CMOS +Cap	1T+1Cst DRAM	2.26	3.1	12	21
CMOS +Cap+TD	1T+1Cst+2TD SRAM	3.15	2.2	12	0.9

Standby current in Table 1 is due to MOSFET leakage in the 6T SRAM cells; in the TD SRAM cells leakage is the sum of MOSFET leakage and TD valley currents; in the DRAM cells standby current is mostly due to bit-line switching during refresh cycles, plus the leakage through the $0.5 \mu\text{m}$ width access transistor. By eliminating the refresh cycle, the embedded CMOS/TD SRAM achieves more than $20\times$ power savings in comparison with embedded DRAM cell.

The TD SRAM cell size is less than half the size of the SRAM cell, with the TD minimum area set by the contact size. An additional mask level would be required to implement this TD SRAM, offset to some extent by a savings in chip area. As a comparison, a 256 Mbit DRAM cell, which uses lithography and patterning comparable to the designs here plus self-aligned contacts and other specialized features, is typically $0.8 \mu\text{m}^2$ or less, but standby current, due to refresh, and due to the back-bias generator, can be several milliamperes. (Back bias is needed in triple-well DRAM arrays to increase the access transistors' threshold voltage and reduce leakage. Higher threshold voltages are not compatible with high-speed logic).

B. CMOS/TD Static Latches and Shift Registers

As in SRAM the TD pair also finds use in CMOS static latches, as shown in Fig. 4. To minimize static power consumption, the TD current is optimized, as outlined in Fig. 5. Too weak a TD current moves the stable point away from the supply rail resulting in an increase in the sub-threshold current of the output inverter; too strong a TD current, on the other hand, increases the standby current of the TD pair.

By cascading the latches in Fig. 4(a), a CMOS/TD static shift register (or D flip flop) is implemented as shown in Fig. 6(a). Here, a complementary pass gate is used to pass the data under the control of the clock signal.

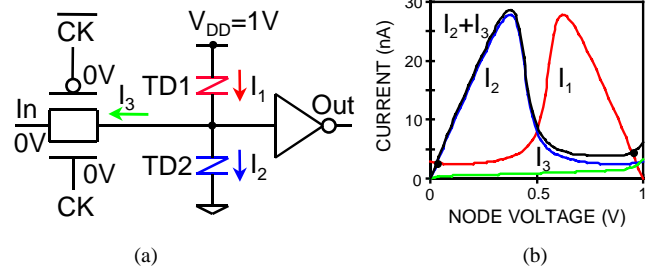


Fig. 4: CMOS/TD static latch: (a) schematic diagram and (b) current-voltage relations.

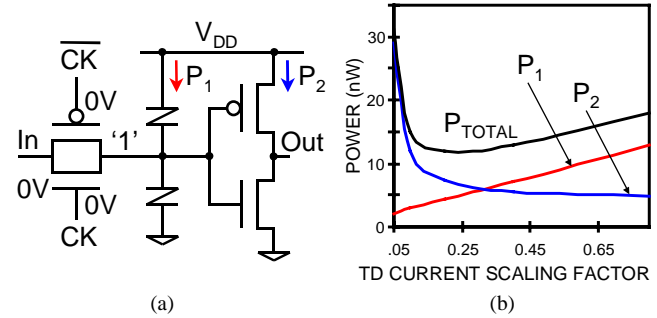


Fig. 5: Static power minimization: (a) schematic diagram and (b) power relationships.

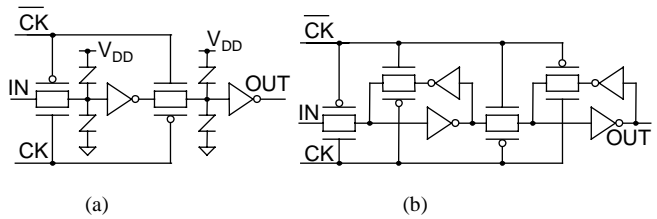


Fig. 6: Static shift register comparison: (a) CMOS/TD and (b) CMOS only.

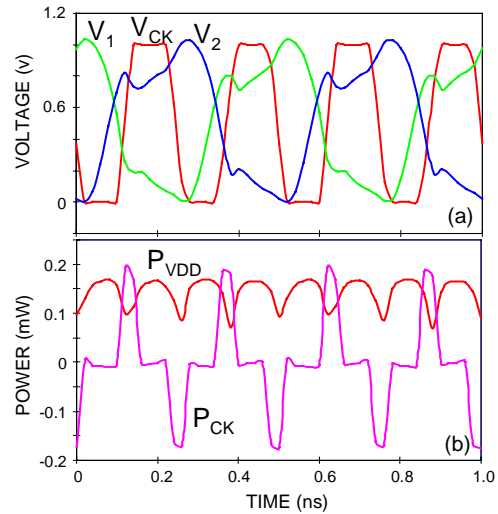


Fig. 7: CMOS/TD static shift register operating at the maximum clock frequency: (a) voltage waveforms and (b) power waveforms.

For comparison, a typical CMOS static shift register with a complementary pass gate is shown in Fig. 6(b). The feedback loop, consisting of an inverter and a complementary pass gate, is used to hold the storage voltage statically.

These circuits were simulated using the models discussed previously; interconnect parasitics were not included. The TD current was optimized to minimize static power consumption. Figure 7 shows the voltage and power waveforms of the CMOS/TD static shift register when operating at its maximum clock frequency. Since two inverters and two pass gates are eliminated, the CMOS/TD shift register has estimated 1.6× smaller area, 1.7× higher speed, and 2.4× lower power in comparison with its' CMOS counterpart, as shown in Fig. 8 and Table 2.

A single clock CMOS/TD static shift register was also similarly designed and compared with its CMOS counterpart, as shown in Fig. 9. The simulation shows that the CMOS/TD single-clock static shift register has estimated 3× smaller area, 2× higher speed, and 2× lower power in comparison with its CMOS counterpart, as shown in Table 3.

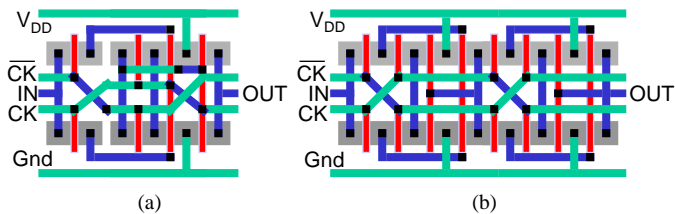


Fig. 8: Symbolic layout comparison of (a) CMOS/TD and CMOS only static shift registers.

TABLE 2
COMPARISON OF CMOS AND CMOS/TD STATIC SHIFT REGISTERS

Process	VDD (V)	Vt (V)	Rel. Area	Max. Clock Rate (GHz)	Active Power (μW/GHz/bit)	Static Power (nW/bit)
CMOS	1.0	0.3	1.6×	2.38	50.0	10
CMOS/TD	1.0	0.3	1.0×	4.00	20.8	16
CMOS	0.5	0.15	1.6×	1.25	14.0	190
CMOS/TD	0.5	0.15	1.0×	2.27	5.7	215

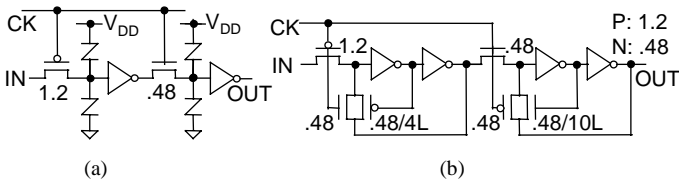


Fig. 9: Comparison of single-clock static shift registers: (a) CMOS/TD and (b) CMOS only.

TABLE 3
COMPARISON OF SINGLE-CLOCK CMOS AND CMOS/TD STATIC SHIFT REGISTERS

Process	VDD (V)	Relative Area	Max. Clock Rate (GHz)	Active Power (μW/GHz/bit)	Static Power (nW/bit)
CMOS	1.0	3×	0.45	27.8	42.0
CMOS/TD	1.0	1×	1.00	13.0	72.0

Conclusions

The technical barriers necessary to use the tunnel diode in conventional IC processes are being removed. We have shown that molecular beam epitaxy can produce uniform and reproducible III-V layers which set the critical peak current and voltage levels precisely across the wafer. We have taken III-V resonant tunneling diode SPICE models and using TI's CMOS models, provided a first look at the benefits of a Si-based TD combined with CMOS. These results show that tunnel diodes can improve circuit performance *without scaling*. Recently demonstrated MBE-grown Si tunnel diodes provide a path to develop this process.

Acknowledgements

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References

- (1) R. G. Swartz, "In perspective: the tunnel diode," *IEEE Int. Solid State Circ. Conf.*, pp. 278-280 (1986).
- (2) A. Seabaugh, et al., "Resonant tunneling circuit technology: has it arrived?" *1997 GaAs IC Symp.*, pp. 199-122.
- (3) A. C. Seabaugh, B. Brar, T. Broekaert, F. Morris, and G. Frazier, "Resonant Tunneling Analog/Mixed Signal Circuit Technology," unpublished.
- (4) T. P. E. Broekaert, et al. "A monolithic 4-bit 2-Gsps resonant tunneling analog-to-digital converter," *IEEE J. Solid State Circ.* **33**, 1342-1349 (1998).
- (5) L. D. Nguyen, L. E. Larson, and U. K. Mishra, "Ultra-high-speed modulation-doped field-effect transistors: a tutorial review," *Proc. IEEE*, **80**, 494-518 (1992).
- (6) N. Shimizu, et al., "In_{0.53}Ga_{0.47}As/AlAs resonant tunneling diodes with switching time of 1.5 ps," *Electronics Lett.*, **31**, 1695-1697 (1995).
- (7) P. van der Wagt, A. Seabaugh, and E. Beam, III, "RTD/HFET low standby power memory cell," *IEEE Electron Dev. Lett.* **19**, 7-9 (1998).
- (8) K. Morita, et al., "High performance CMOS compatible bistable operation at extremely low supply voltage by a novel Si interband tunnel diode," *56th Dev. Res. Conf.*, pp. 42-43 (1998).
- (9) S. L. Rommel, et al., "Room temperature operation of epitaxially grown Si/Si_{0.5}Ge_{0.5}/Si resonant interband tunneling diodes," *Appl. Phys. Lett* in press.
- (10) P. van der Wagt, *Proc. IEEE*, in press.