CMOS RF Power Amplifier Design for Wireless Communications

In recent years, there has been great technology improvement in wireless communication systems. Novel transceiver architectures and circuits have enabled faster data transfer rates over larger areas, while burning even less power. CMOS technology, by its unique advantages in costing and integration, has enabled an unprecedented level of integration in modern low-cost, small form-factor and low-power wireless devices. The two of them put together has made our phones, our mp3 players, etc., smarter and smaller, and most importantly, has made our lives more pleasant.

There have been great efforts contributed to integrating the whole transceiver into one single CMOS die. However, RF Power Amplifiers (PAs) are still among those few remaining modules that have yet to be successfully integrated. The reduced supply voltage, high on-chip passive losses, and the low breakdown voltage of the thin gate oxide CMOS devices are among the most difficult challenges, which have forced high output power CMOS PAs to operate under large-current, low-impedance levels where they are vulnerable to parasitic losses. On the other hand, efficiency is another big concern in PA designs. Due to the inevitable power back-off in modern communication systems, it is of great importance to improve the efficiency of a PA when it does not work at its maximum rated power. This presentation addresses two major issues, namely power combining and average efficiency enhancement. By utilizing on-chip transformers and adaptive load techniques, we observe an improved efficiency over a wide input range in our proposed PA prototype. And to the author’s knowledge, the prototype has the most efficiency recovery points among today’s reported fully integrated CMOS PAs. Some related extended research results including Nano-particle Magnetic-cored Inductor (NMI), NMI/graphene inductor Voltage Controlled Oscillators (VCOs) and a pHEMT SP4T RF switch will also be presented in the talk.