College of Engineering<br>University of California, Riverside<br>EE134<br>Final Project: 4-BIT ADDER<br>3-20-03

Team 4
Dustin Jameson
Ronald Alfonso
Chris Tiu

## Introduction:

Our project for this class is to design and implement a 4-bit adder at the transistor level, using of Cadence software we will do this. After calculating the truth table for the adder, we are to draw a logic gate diagram, stating which logic gates will be used. After which, we will then draw the Transistor schematic of the adder. Finally we will then create a layout for each of the logic gates, then combining them in a single layout to complete the design process of the adder. Once this is completed, we are to have the chip fabricated by connecting the adder to the pad frame and then sent to MOSIS to be constructed.

## Procedure:

Using the following block diagram for a 1-bit adder we will construct a 4-bit adder by carrying the Cout into the Cin of the next adder. Thus there will be a parallel input for bits A (4-bits), B (4-bits), and Carry-in, or Cin (1-bit) giving a total of 9 inputs. There will be 5 outputs S (4-bits) and a Cout bit. First we need to construct the logic gates required by the schematic below. These inputs and outputs combined will give a total of 14 pins not including the 2 pins for power and ground.


Full Adder

| A | B | Cin | SUM | Cout |
| :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

## Gate Schematics:

The following includes the NAND2 and XOR2 gates that needed to be constructed to build the 4-bit adder. Included are the truth tables and schematics and layouts for each.

NAND2:


| $\mathbf{A}$ | $\mathbf{B}$ | $\mathbf{Y}$ |
| :---: | :---: | :---: |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |



XOR2:


| A | B | Y |
| :--- | :--- | :--- |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




## 2. Logic Gate schematic

Once the truth table and logic equations have been simplified. We can now proceed to the next step, which is the logic gate schematic. Here we apply the equations obtained from the truth table, in order to draw out the corresponding logic gate schematic. In this case, we can just one full adder schematic, and then repeat the process three more times in order to complete the 4-bit adder circuit. A picture of our circuit is attached on a separate sheet of paper.


## 3. Transistor-level schematic

After the completion of the Logic Gate Schematic, we then assemble the schematic in terms of transistors, p-mos, and n-mos transistors.


## 4. Layout Schematic:



## Padframe:



Pinout:


## Testing:

To test this chip one needs to supply a high or low to bits A (4-bits), B (4-bits), and the Carry-in. If one were to input $\mathrm{A} 0=1, \mathrm{~B} 0=1, \mathrm{Cin}=0$, the following output would be S 1 $=1$, which would mean 2 . Also don't forget to connect the power and ground!

